Testing of Complex Digital Chips

Juri Schmidt
Chair of Computer Architecture, Institute for Computer Engineering
University of Heidelberg
Mannheim, Germany
juri.schmidt@stud.uni-heidelberg.de

***Abstract*—This paper describes the common methods to test a chip after the fabrication process for manufacturing faults and shows the best trade off between testing on wafer level and after packaging depending on yield and quantity of fabricated dies. Further, advice on reducing test cost is given. As an outlook, a technology on wafer probe cards that might come up and gain importance in the future is presented.**

***Index Terms*—ASIC Test, Chip Test, Wafer Level Test, Package Level Test, Design For Testability, Test Cost Reduction, Probe Card.**

February 11, 2013

I. Introduction

Evolution in manufacturing technology, especially smaller feature sizes, denser ICs, higher operating speeds and larger silicon wafers, are huge challenges for the semiconductor industry. A higher density also means higher probability for defective parts per area. Smaller feature sizes, down to estimated 10nm in 2020 [1], raise the probability of defects, for example on thin gates. Without the possibility to detect defective dies, these parts would reach the end user, of course with a negative impact on reputation, credibility and costs for replacing defective chips in field. This is where the industry makes use of fabrication, namely wafer level and package level, tests. Testing a chip is crucial, although it adds costs to the design flow without any visible results to the end user. This paper shall clarify the need for chip testing and its increasing importance with the progress in semiconductor technology. At first chapter II introduces and analyses the methodology of Design for Test. The various methods with their advantages and disadvantages for testing a chip on wafer level shall be presented in chapter III. Finally, chapter IV trades off test against the resulting costs and gives advice, when it is beneficial to enable wafer level testing instead of testing a chip only in package.

II. Design For Testability

As mentioned before, testing chips becomes more difficult with higher logic density, higher I/O pad count and shrinking pitch. New test methods, where testing is considered in the early design phase, were introduced in the early 1970s [2]. The process of adding dedicated test functionality to allow wafer level testing is referred to as Design for Testability (DFT). Additional test logic is inserted into the integrated circuit. In the following, two test methods are introduced. The first one tests logic whereas the so called Boundary Scan checks the correctness of on-die I/O cells and the interconnect between the die and the PCB where the it will be mounted.

A. Scan Design

While there are many reasons for manufacturing faults in an integrated circuit, they can be divided into several fault models. The two most common are Stuck-at and Dynamic fault models [3]. However, a scan design allows to test a die for faults without knowledge of the logical purpose. Each flip flop (FF) in a sequential path is replaced by a so called Scan-Flip-Flop. These Scan-FF have an additional input, the so called scan in. The flip-flops are then connected as a scan chain in series. This means that each output of a FF is connected to the scan input of the following. Now a serial test pattern can be applied at the input of the first FF in the chain. Insertion of Scan-FF makes all sequential and combinational logic in between observable. Note that a scan design performs checks on the pure logic independent from the logical function. Functional testing is time consuming and should be performed before fabrication, because time on a Wafer Level Tester is expensive.

B. Boundary Scan

The Joint Test Action Group (JTAG) developed a boundary scan standard in 1990 [4]. Boundary Scan, that is additional logic that is inserted into the design to detect faults in the interconnect between the die and the PCB. Dies with boundary scan provide access through a four-wire serial bus called test access port (TAP) [5]. Test data and instructions can be applied to the die and the I/O pads. On the PCB, the various signals are probed and compared to the test vector applied at the TAP. To specify the behavior of a device during boundary scan, the boundary scan description language (BSDL) was introduced [6].

C. Disadvantage of DFT

The biggest disadvantage of Design for Test is the additional logic with the need for more chip area, because every flip-flop in the chain needs an additional multiplexer to switch between normal and test input. Therefore DFT is critical to area-limited chips, but should always be considered because DFT becomes even more important with higher logic count.

III. Test Hardware

To facilitate wafer level testing the I/O pads of a die, which is also called the device under test or simply DUT,

must be contacted. For this purpose so called probe cards were developed. These probe cards adapt the fine pitch of a die to a more coarse one, providing an interface between an Automated Test Equipment (ATE) and the die itself. Besides conventional, needle-based probe cards, so called Membrane Probe Cards were developed. Advantages and disadvantages will be discussed in this chapter. Note that physical probing always needs electrical contacts between the die and the probe card. This leaves marks on the I/O pads and may complicate pad bonding or even damage the chip. A solution to enable Wafer Level Testing without contacting the I/O pads physically is presented in section III-D.

A. Cantilever Needle Probe Cards

Cantilever needle, also known as horizontal probe cards have been around for decades. Many probe tips are mounted along a ring, having a spring characteristic in the range of 50 to 100 μm to eliminate irregularities on either the wafer or the tips [7]. They are a cost effective solution for many applications. The horizontal movement on the wafer provides pad scrubbing and makes a good electrical contact to up to 2000 pads [8]. Debris on the wafer and/or the I/O pads can contaminate the probe tips. However, problems arise with a higher density of I/O pads and/or a smaller pitch which makes alignment and cleaning of the fine probe tips harder. Further the size of the probe tips and the resulting parasitic conductance may limit high speed testing capabilities up to a maximum of 400MHz [8]. Special RF Cantilever Needle Cards allow frequencies up to 4GHz, with increased test costs, of course. Again, physical probing of I/O pads always leaves a mark. To reduce the chance for damaging a pad the needles or probe tips consist of micro-springs. This reduces the pressure on each pad and enables the elimination of irregularities, as mentioned before. Cantilever needle cards can be used for either perimeter or in-line pad layout [9].

B. Vertical Probe Cards

Vertical probe cards can be divided into several types. The most important and most common type consists of an array of pins, allowing up to 5000 probes [8]. The probe card is led vertically, contrary to horizontal probe cards, onto the die. This enables especially the testing of dies with area I/O pads and at speed functional tests up to 5GHz [8], because the pin inductance is kept to a minimum. Further vertical probing leaves significantly smaller probe marks or, in the case of an area array flip chip design, less deformation of the solder balls. This reduces the chance to damage DUT pads (see figure 1). On the other hand, vertical probe cards are significantly more expensive than the horizontal ones. They should be used for area array pad layout only.

Fig. 1: Probe Marks: Horizontal (left) vs. Vertical Probing [10]

C. Membrane Probe Cards

The membrane probe card, developed by Hewlett Packard Co. in 1988 [11], is made up of a flexible dielectric membrane featuring highest bandwidth up to 20GHz [10]. This membrane contains lithographically defined transmission lines on the top. Up to 800 contacts [8] to a DUT are made through holes in these transmission lines. Crosstalk is kept low compared to needle based probe types. Irregularities on the DUT pads are eliminated due to the flexibility of the membrane. Positional accuracy is reached by simply forming the membrane. Membrane probe cards can be used for all types of pad layout if there are not too many pads.

D. EMWS Technology [12] [13]

The EMWS (ElectroMagnetic Wafer Sort) technology allows fully contactless wafer testing. A radio antenna in the die allows communication with the ATE, dedicated test I/O pads will become needless, therefore reducing the die size. Low power ICs may be tested fully contactless, saving costs for probe cards and maintenance. Higher power ICs still require probes to contact power and ground to the die. Even the yield may be increased because there is no chance to damage chips through probe marks anymore. Further EMWS enables full parallel testing up to the whole wafer at one time and at speed. The industries research in this direction is ongoing.

IV. Process Analysis

Now that the various methods to test a chip on wafer level have been presented, the most cost effective way to test a chip shall be found. In order to do so, many parameters have to be taken into account. First of all the entire costs must be split into two parts. The non recurring engineering costs (NRE) and the costs per unit. The NRE costs are fixed for each step in a design process. The costs per unit will be discussed later in this chapter. To estimate the overall yield a few variables are introduced in table I.

Variable	Definition
GDW	Number of dies that can be cut out of a wafer
D_W	Number of dies tested during wafer test
W	The number of wafers produced
D_P	Non defective dies. These will be packaged
Y_{WT}	The yield achieved during wafer test
Y_{PT}	The yield achieved during package test
KGD	Number of fully tested and operational dies
Y	Overall yield

TABLE I: Parameters for Yield Calculation [14]

Assuming that the number of dies that can be cut out of wafer is fixed, the number of dies that is gained from W wafers is

$$D_W = GDW * W$$

Some of these dies will be discarded during wafer level test. Depending on the yield the total number of dies that will be packaged is

$$D_P = D_W * Y_{WT}$$

Having another yield at package testing the number of known good dies (KGD) decreases further. It is the product of the number of dies packaged with the package testing yield Y_{PT}:

$$KGD = D_P * Y_{PT}$$

The overall yield is now the amount of KGD divided by cut out dies (GDW):

$$Y = \frac{KGD}{D_W}$$

or simply the product of both, the wafer level and the package yield:

$$Y = Y_{WT} * Y_{PT}$$

The resulting overall yield is crucial to find the most cost effective way for chip testing. As the yield affects the test costs, the next step is to calculate the overall costs as a function of the yield respectively the known good dies (KGD). Again some variables are introduced in table II. The total cost TC

Variable	Definition
C_{WT}	The cost of testing a die at wafer test
C_{PT}	The cost of testing a die at package test
C_P	The cost of packaging a single die
NRE_{WT}	NRE costs of wafer test
NRE_PT	NRE costs of package test
NRE_P	NRE costs of package development
TC_{WT}	Total cost of wafer test
TC_{PT}	Total cost of package test
TC_P	Total cost of packaging
TC	Total test cost

TABLE II: Parameters for Cost Calculation [14]

consists of three sub-components. The cost for wafer level test, package test and the packaging itself. The total cost of wafer testing is defined as

$$TC_{WT} = D_W * C_{WT} + NRE_{WT}$$

In analogy to wafer level testing, the cost for package testing is

$$TC_{PT} = D_P * C_{PT} + NRE_{PT}$$

Cost for packaging:

$$TC_P = D_P * C_P + NRE_P$$

The total cost TC is defined as the sum of these three components:

$$TC = TC_{WT} + TC_{PT} + TC_P$$

As a function of KGD the most cost effective way can be calculated with

$$Cost = \frac{KGD}{Y_{PT}}(C_{PT} + C_P) + \frac{KGD}{Y_{PT}Y_{WT}}C_{WT} + \sum NRE$$

Now, summing up all parameters it is clear that a general conclusion on an optimal test strategy can not be made. Instead, the best strategy may be calculated individually. In the following a test scenario shall be demonstrated. At first the parameters must be filled with some reasonable values as shown in table III.

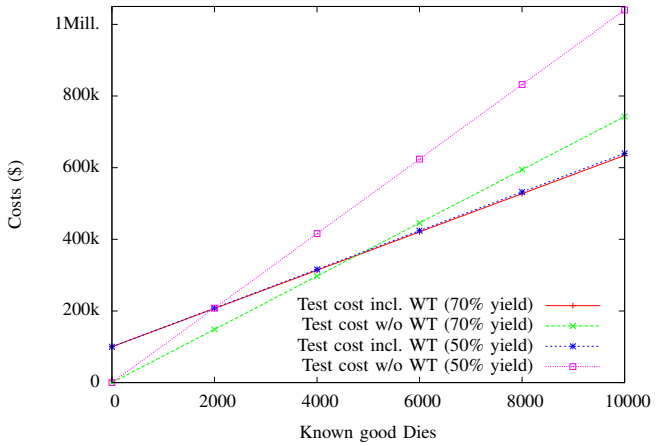

Fig. 2: Wafer level vs. Packaged testing costs

Parameter	Value in $
C_{WT}	1
C_{PT}	2
C_P	50
NRE_{WT}	100.000

TABLE III: Parameters for a Test Scenario

Figure 2 shows the trend for two different yields over a raising amount of dies starting with zero, each with and without a wafer level test phase. The NRE costs for packaging and the test environment for packaged dies occur in all cases and will be neglected. As stated in chapter III, wafer level testing needs maintenance in the form of cleaning and realignment of the probe needles from time to time. For simplification, these costs are disregarded as well.

It is important to note that these assumed values are only estimations and may vary for different packages, structure sizes or I/O-counts, which affect the complexity of probe cards in wafer level testing and therefore raise the costs of NRE. At a first glance it may be confusing that testing a chip in package is more expensive than a test on wafer level. Besides the high NRE costs for wafer level testing, it has some advantages concerning the test time over packaged testing. Fully automated test equipment may test a bunch of chips at a time in parallel, even faster than a single die in a package test environment.

As figure 2 shows there is a turning point when one test approach becomes cheaper than the other. In other words, the intersection shows when testing on both, wafer and package level, becomes cheaper than testing only in package. For given wafer test and package test yields this "Turning Point of Known Good Dies (KGD_X)" can be calculated with

$$KGD_X = \frac{NRE_{WT}}{(C_{PT} + C_P)(\frac{1}{Y_{PT2}} - \frac{1}{Y_{PT1}}) - \frac{C_{WT}}{Y_{PT1}Y_{WT}}}$$

where Y_{PT1} is the package test yield after wafer level testing and Y_{PT2} is the package test yield when only package testing is performed. Note that Y_{PT1} is significantly higher than Y_{PT2}

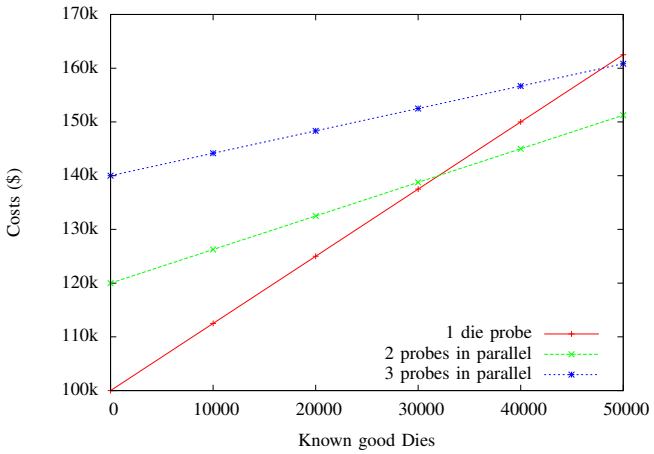

Fig. 3: Parallel Wafer Level Test: Yield = 80%

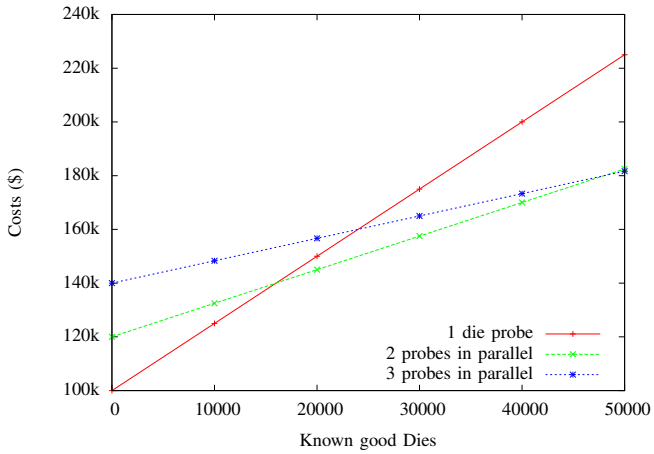

Fig. 4: Parallel Wafer Level Test: Yield = 40%

because most of the defective chips were sorted out during wafer level test.

For the presented example the point when wafer level test should be used is at 2000 known good dies (50% yield). Note that the higher the yield gets, the more this point moves to the right. Having a yield of 70% it is at 4930 KGD already.

A. Test Cost Reduction

The overall process costs consist of wafer level and package test costs. The cost for wafer level testing is made up of the NRE and the time needed to test a single die. Package test costs mainly include the NRE and maintenance of test hardware. There may be technologies in the future that affect all these parameters in a good manner, refer to chapter III-D.

However, one approach to reduce the costs is the use of parallel die testing, which can affect the overall costs in a beneficial manner. This approach strongly depends on the yield and the quantity of fabricated chips. Figure 3 and 4 show the cost progress for parallel testing with 80% respectively 40% yield. The NRE costs can be assumed with $100.000 for test equipment including one die probe. Each additional die probe requires an extra charge of $20.000. The average time to test a single die scales with the rank of parallelization and therefore reduces the cost Y_{WT} of testing a single part on wafer level by the same factor. Note that the maintenance costs are not included, but will rise for each additional die probe. For calculation, three new parameters are introduced in table IV.

Parameter	Description
PAR	Rank of parallelization (amount of die probes)
CNT_{WP}	Amount of additional die probes ($\hat{=}$PAR-1)
C_{WP}	Cost per additional die probe

TABLE IV: Parameters for Parallel Wafer Test

The overall costs for parallel testing are calculated with

$$\text{Cost} = \frac{\text{KGD}}{Y_{PT} * Y_{WT}} * \frac{C_{WT}}{\text{PAR}} + \text{NRE}_{WT} + \text{CNT}_{WP} * C_{WP}$$

Another possibility to reduce the test costs is to keep the time for maintenance of the test hardware to an absolute minimum. The industry therefore expends a lot effort on the research in this direction, the use of new materials for example.

V. Conclusion

As stated in chapter IV, an easy decision on the test approach cannot be made. Instead many parameters have to be taken into account. This results in an individual ”best” approach depending on the yield, the quantity of fabricated dies and so forth. Generally it can be said that the importance of wafer level testing rises with shrinking overall yield. Furthermore figure 2 shows that there may be a point when enabling wafer level test should be preferred to testing chips only in package. Due to the fact that fewer defective chips will be packaged and assembled, the cost for these steps can be reduced significantly. Further cost reduction may be reached with advances in process or additional test logic as discussed in chapter IV-A resp. chapter II. In addition, enabling wafer testing gives feedback on the overall status of the fabrication process, so that this process may be refined by the manufacturer. Choosing the proper type of probe card is another crucial factor in cost saving. While needle-based probes are relatively cheap they need a lot of alignment and maintenance such as cleaning. The narrow bandwidth is a strong limitation too. Vertical probe cards extend the bandwidth with less maintenance. But this type is significantly more expensive. Membrane technology enables highest bandwidth with minimal stress to the I/O pads. The limitations here are the number of I/O pads and the high price.

Acknowledgment

The author would like to thank each employee of the Chair of Computer Architecture, Institute of Computer Engineering, University of Heidelberg, who helped me to write this paper. Special acknowledge goes to Professor Ulrich Bruening, head of the Chair of Computer Architecture, for his assistance and the hosting of this research.

REFERENCES

[1] International Roadmap For Semiconductors, *2011 Edition, Executive Summary* 2011

[2] Yinghua Min and Charles Stroud, *VLSI Test Principles and Architectures: Design for Testability* Chapter 1, San Francisco, 2006

[3] Markus Mueller, *Exploring the Testability Methodology and the Development of Test and Debug Functions for a Complex Network ASIC* Chair of Computer Architecture, University of Heidelberg, Mannheim, Aug. 01, 2011

[4] IEEE Std. 1149.6-2003, *IEEE Standard for Boundary-Scan Testing of Advance Digital Networks* Institute of Electrical and Electronics Engineers, New York, 2003

[5] IEEE Std. 1149.1-2001, *IEEE Standard Test Access Port and Boundary Scan Architecture* Institute of Electrical and Electronics Engineers, New York, 2001

[6] K. P. Parker, *The Boundary-Scan Handbook* Kluwer Academic, Norwell, MA, 2001

[7] Julia Goldstein, *Probe cards enable wafer level test* http://www.electroiq.com/articles/ap/print/volume-14/issue-12/features/probe-cards-enable-wafer-level-test.html, last visited Jan. 22, 2013

[8] Martin Dresler, Frank Goh, Eng-Keong Tan, *Parallel RF Wafer Sort Production Testing* Jan. 14, 2009

[9] William Mann *"Leading Edge" of Wafer Level Testing* Chair, Southwest Test Workshop, 2004

[10] William R. Mann, Frederick L. Taber, Philip W. Seitzer and Jerry J. Broz *The Leading Edge of Production Wafer Probe Test Technology* Paper for IEEE International Test Conference, Charlotte, NC, 2004

[11] Brian Leslie and Farid Matta, *Membrane Probe Card Technology* Paper for IEEE International Test Conference, Hewlett Packard Co. R&D Laboratories, 1988

[12] STMicroelectronics, *Worlds First Fully Contactless Wafer Test* http://www.st.com/internet/com/press_release/t3256.jsp, last visited Jan. 17, 2013

[13] Dae Young Lee, David D. Wentzloff and John P. Hayes *Wireless Wafer-Level Testing of Integrated Circuits via Capacitively-Coupled Channels* Department of Electrical Engineering and Computer Science, University of Michigan, 2011

[14] S. Kapferer, *Methodology and Ecosystem for the Design of a Complex Network ASIC* Dissertation, University of Mannheim, 2012