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HEIDELBERG

Testing of Complex Digital Chips

Juri Schmidt

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Outline

- Motivation
  - Why testing is necessary
- Background
  - Chip manufacturing
  - Yield
- Reasons for ‘bad’ Chips
- Design for Testability (DFT)
- Wafer Level Test Hardware
- The best test strategy
  - Wafer Level vs. Package Test
  - Cost analysis

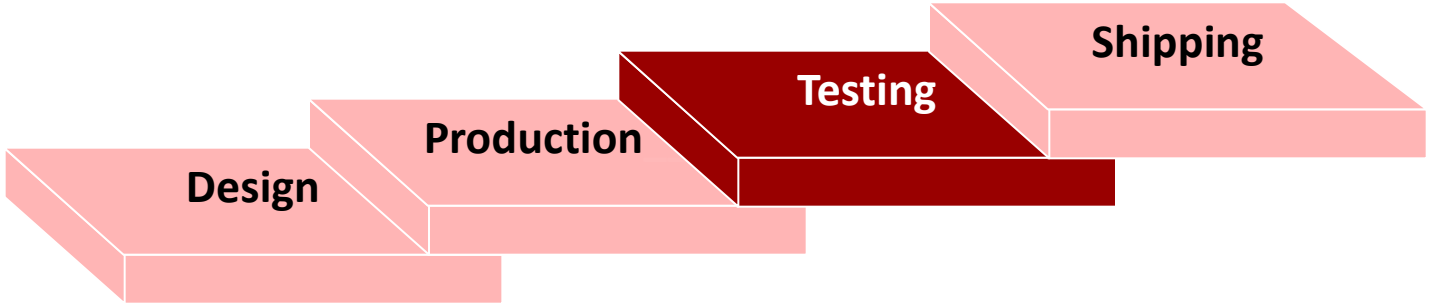
Motivation

Testing is …to check wether a chip behaves correctly

- Manufacturing tests: between production and shipping

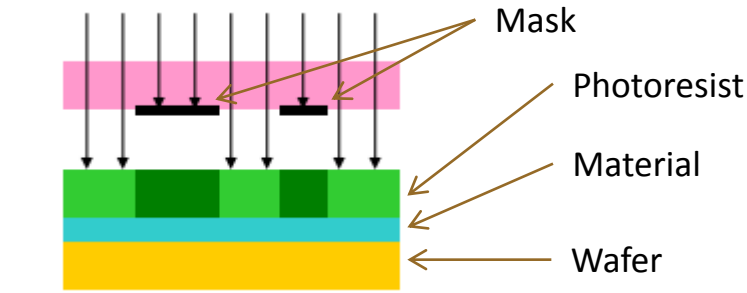
Reveal faulty Chips

- Increase quality of product
- Raise reputation / credibility
- Maximize Yield
- Reduce Costs (especially replacement in field)



Chip manufacturing - Process

- Photolitography
  - Resolution is limited by the light source
    - 193nm for UV
    - 13.5nm for E-UV using mirrors
  - Many layers
    - 4 to 10 metal + isolator each



Photolitography Step[1]

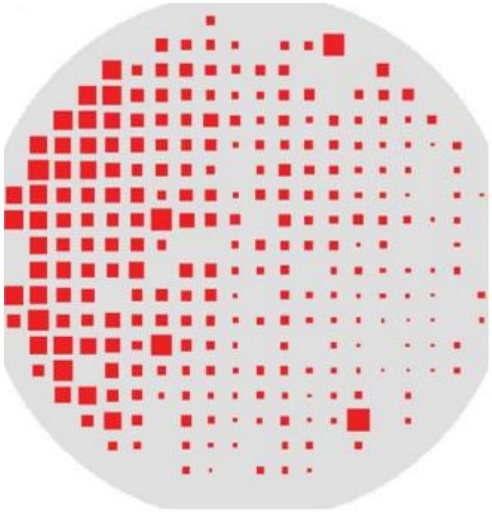
- Process takes approx. 6 to 8 weeks
  - ➢ Wafer with diameter of 100 to 300mm

Chip Manufacturing - Yield

- Yield is defined as:

$$\frac{\text{number of good chips on a wafer}}{\text{total number of chips}}$$

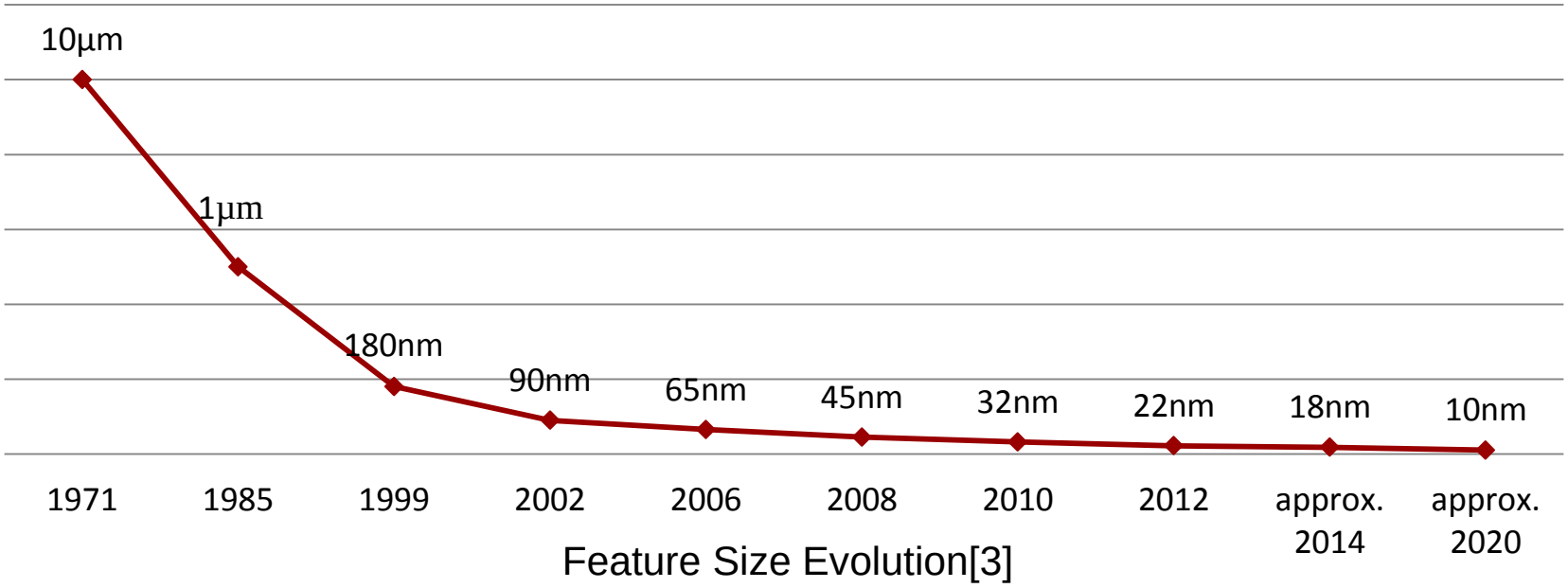
- Example:
  - a yield of 0.5 50% “good” chips



example “good” chip distribution [2]

Chip Manufacturing – Feature Size

- Yield decreases with feature size reduction
  - More transistors per die increase the possibility for defects



Reasons for Bad Chips

Variation in Process

- Transistor channel length
- Transistor threshold voltage
- Metal interconnect width and thickness

Impact on the speed of a chip

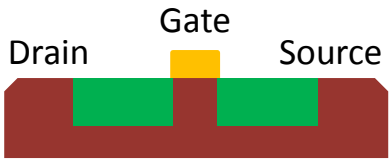
Disturbances in Manufacturing

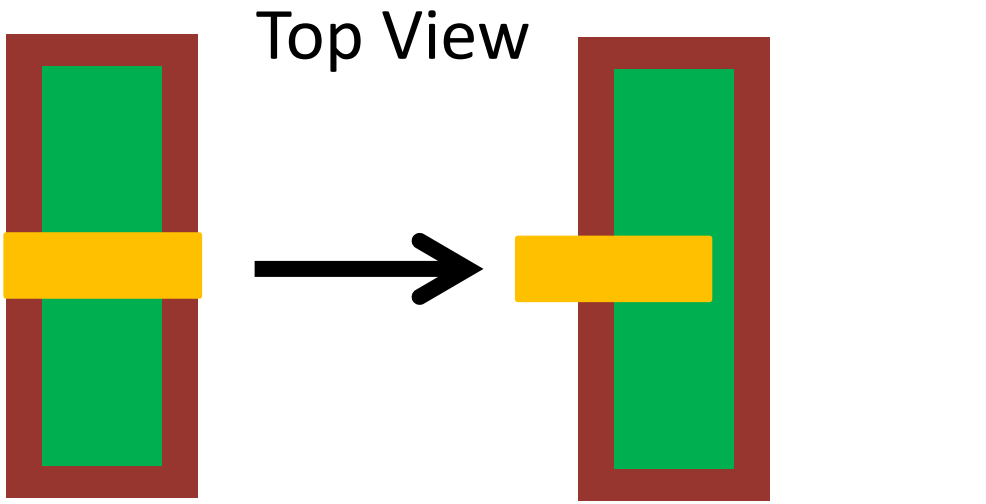
- Temperature
- Humidity
- Vibrations
- Light
- Dust
- Electrostatic Charge
- Purity of Materials
- Misaligned Masks

Can harm single dies up to whole wafer

Mask misalignment

- Can cause shorts / open circuits



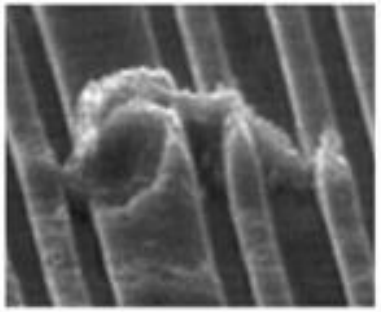


Good!

Fatal ! Short in Drain/Source

Fault class: Static defects

- Layer to layer shorts
  - e.g. metal to metal or V_{DD} to GND
- Discontinuous wires
  - floating inputs, disconnected outputs
- Shorts in oxide
  - e.g. gate connected to V_{DD}

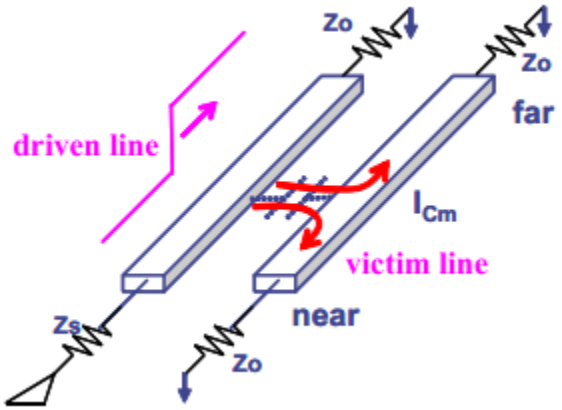


Shorted Circuit [4]

Open Circuit [4]

Fault class: Dynamic defects

- Dynamic defects
  - Only appear under certain circumstances
  - For example: high frequency
- Typical:
  - Timing violation / Delay
  - Crosstalk
  - Noise



Crosstalk[5]

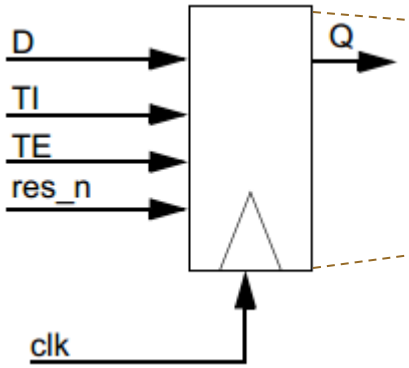
- Hard to test, chip needs to run in normal operation
  - ➢ Simulation of crosstalk or other effects

Design For Testability (DFT)

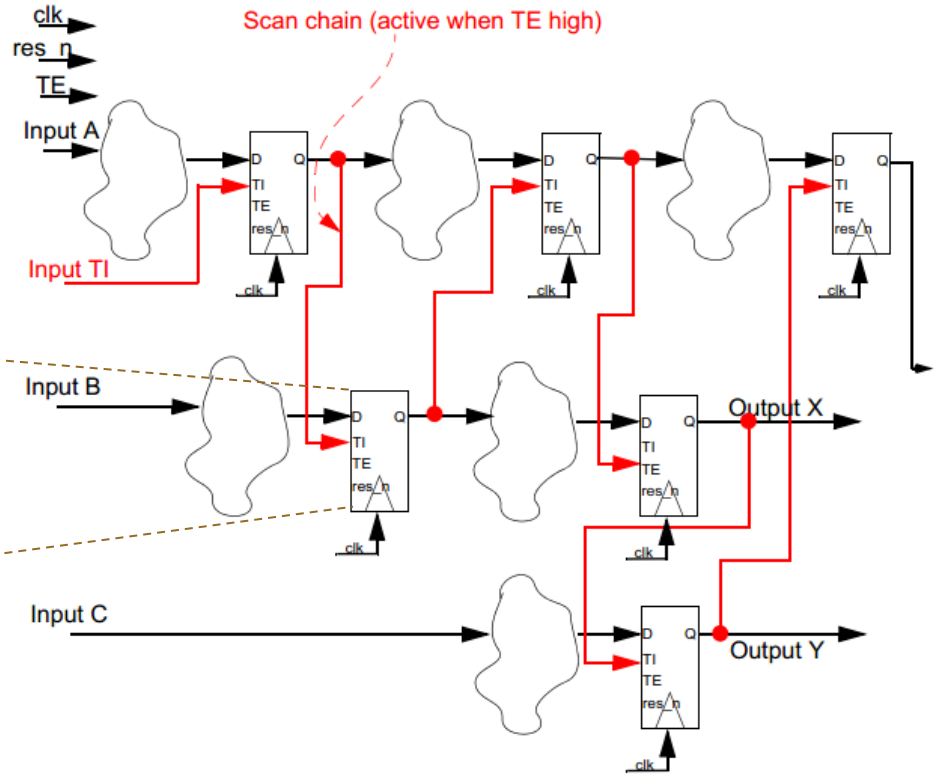
- Insert dedicated test functionality to allow Wafer Level and Package Testing
  - All logic becomes observable
  - Apply Serial Test Pattern
- Checks logic itself, NOT functional verification
  - FV is time consuming
  - Test time is expensive
- Importance of DFT rises with higher logic density
  - More logic → Higher fault probability

DFT: Scan chains

- Output (Q) of FF is Test-Input (TI) of the following one
- Impact on:
  - Area
  - Delay (Critical Paths)



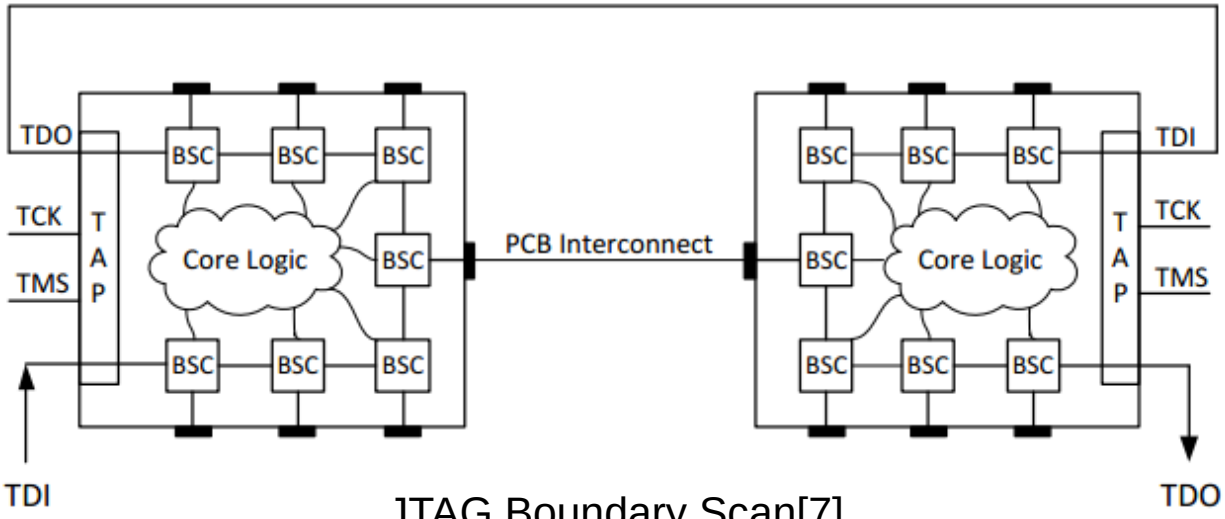
Scan FF [6]



Scan chain [6]

DFT: Boundary Scan

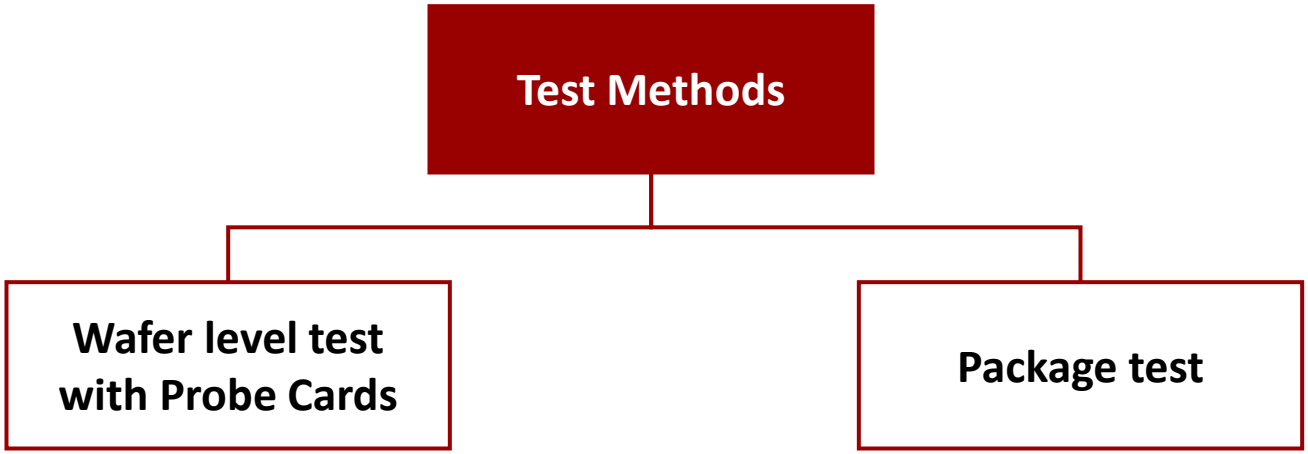
- Introduced by Joint Test Action Group [7]
- Access through 4-wire serial test access port (TAP)
- Test for:
  - I/O Cells
  - Interconnects between chip and PCB



JTAG Boundary Scan[7]

Test methods

For testing, on-chip I/O-pads must be contacted:



- Traditional, physically contacted
  - Horizontal, Cantilever Needle
  - Vertical
  - Membrane
- No or few physical contacts, Wireless
  - EMWS

- Test in Socket

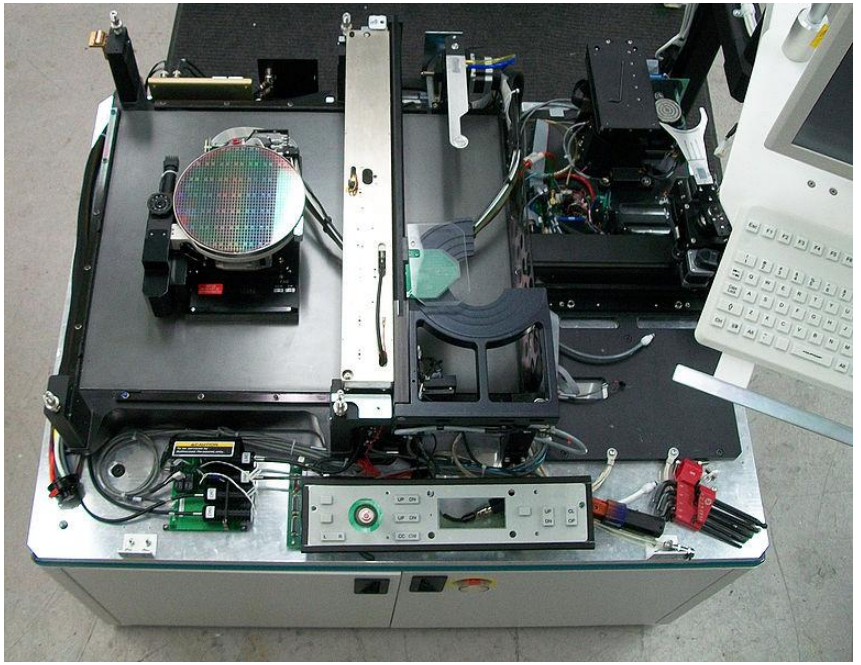
Test Hardware: ATE

Automated Test Equipment (ATE)

- Contains the tester and a probe card
- Tester applies a test pattern
- Measuring & Monitoring

If a die does not pass all tests it is discarded or will be used as lower cost part

- e.g. Intel Celeron, defective Cache is simply reduced

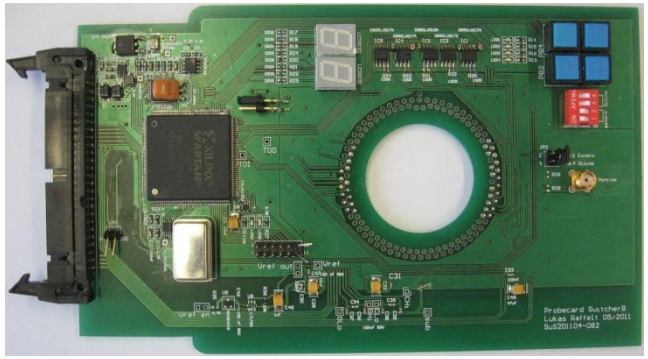


Automated Test Equipment[8]

Probe Cards

- What is a Probe Card
  - Interface between tester and device under test (DUT)
    - Apply fine pitch of I/O pads to the ATE
  - Consists of a PCB and contact elements
  - Adapts to the probe station
  - Different types and technologies
    - Depends on costs and purpose

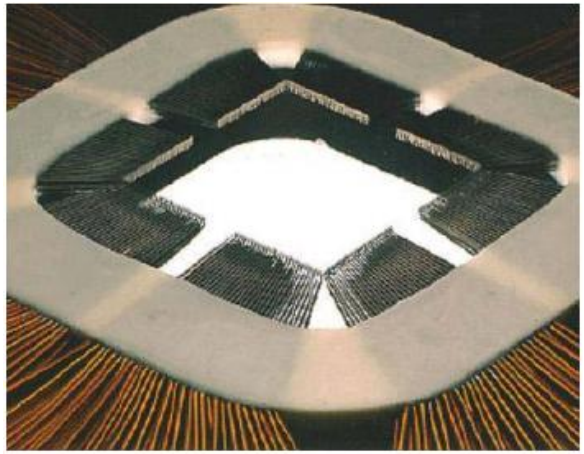
Probe Card



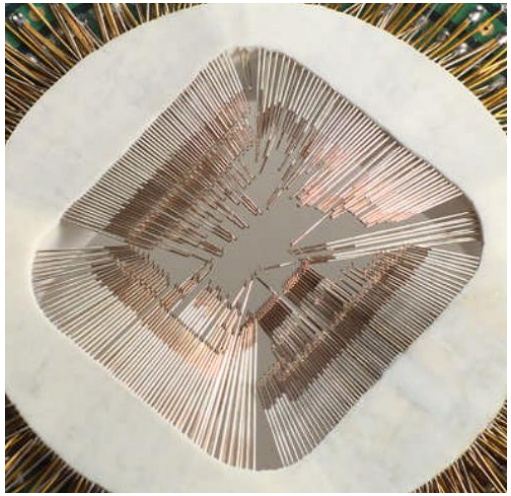
Probe Card PCB

Probe Cards: Horizontal

- Cantilever needle probe cards
  - Probe needles on I/O Pads
  - Good contact through horizontal scrubbing
- Features
  - \+ Relatively cheap
  - – Alignment is difficult
  - – Parasitic inductance
  - – Needles must be maintained
    - Difficult for increasing pin count
  - – Can leave significant probe marks
    - Spring characteristic decreases probability to harm I/O pads



Cantilever needle probe[10]

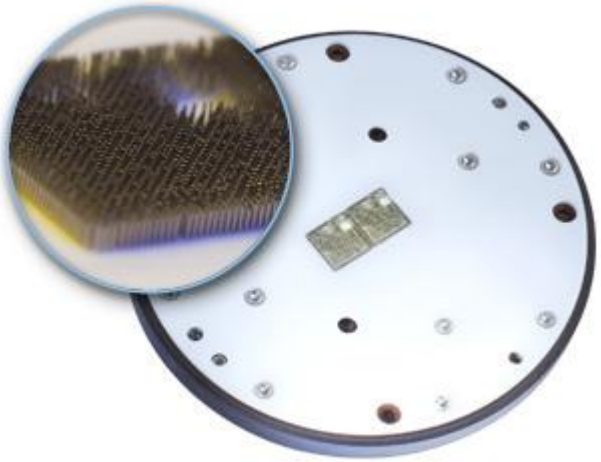


Cantilever needle for area IO [10]

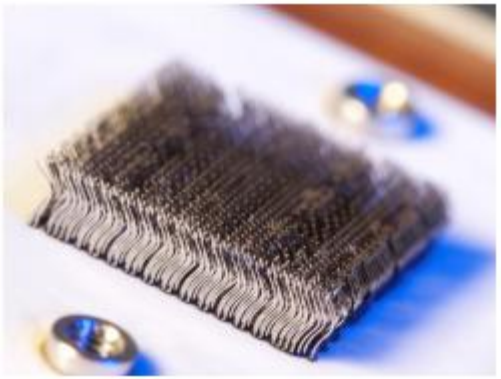
Probe Cards: Vertical

- Vertical probe cards
  - Array of pins
  - Especially for area-I/O

- Features
  - \+ Higher frequencies (up to 5GHz)
  - \+ Up to 5000 pads
  - \+ Smaller probe marks
  - \+ Lower inductance than Cantilever Needle but …
  - – More expensive !



Vertical Probe card[10]

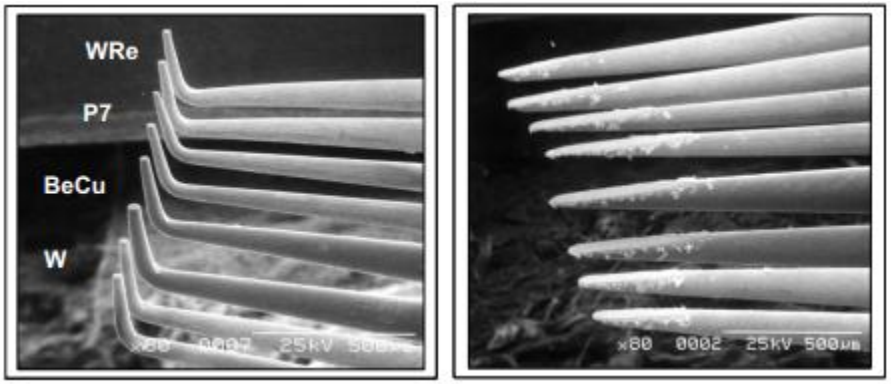


Vertical Probe – Contact elements[11]

Test Hardware: Problems

- Problems for Needle based probe cards:
  - Mechanical contacts may damage pads on IC
    - This can cause wire bond failures
  - Debris contaminates probe tips
    - Must be cleaned!
  - Alignment is difficult

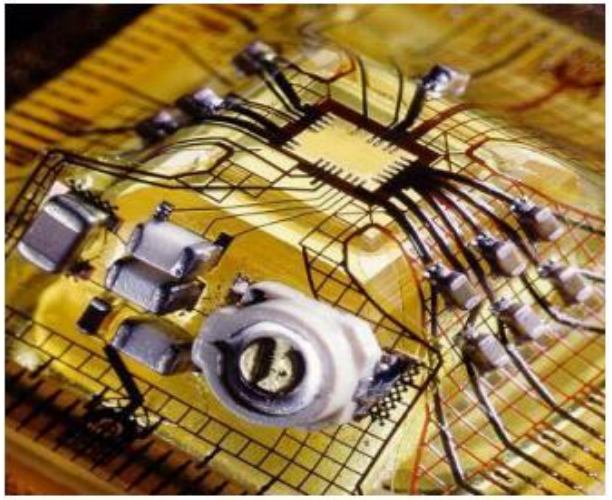
Probe mark[12]



Probe Tips - cleaning[13]

Probe Cards: Membrane

- Membrane technology
  - Flexible Membrane
  - Transmission lines, litographically defined
  - Contacts through holes in trans. lines
- Features
  - \+ High frequencies (up to 20GHz)
  - \+ Very low inductance
  - \+ Easy alignment
  - – High Price
- Limitation
  - Pad Count



Membrane Probe Technology[13]

Wafer Level vs. Package Testing

Wafer Level

- High initial costs (NRE)
  - about $100.000
- Reject defective devices at this early stage:
  - avoid costs for unnecessary packaging
- Test data provides overall status on the fabrication process

Package

- No special equipment needed
- Last chance to detect faulty chips!
- Costs increase with:
  - chips fabricated
  - decreasing yield

Note: **A tradeoff between test coverage and acceptable defects is very important!**
The best test strategy has to be determined individually

Wafer Level vs. Package Testing: Costs

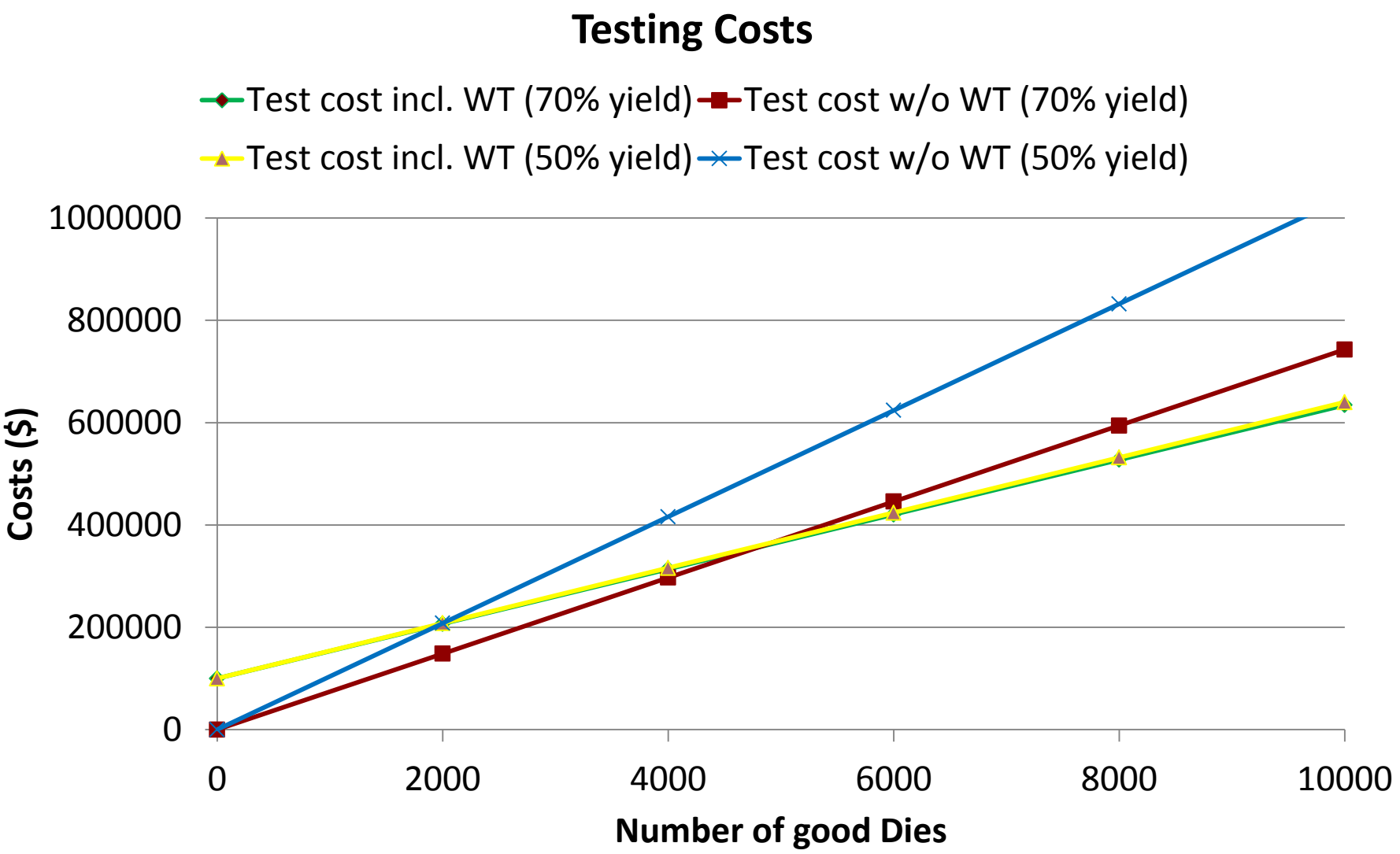
$$\text{Test Cost} = \overset{1}{\frac{KGD}{Y_{PT}Y_{WT}}} C_{WT} + \overset{2}{\frac{KGD}{Y_{PT}}} (C_{PT} + CP) + \overset{3}{\sum} \text{NRE}$$

1. Overall Dies produced and tested on Wafer Level
2. Dies packaged and tested in Package
3. Overall Non recurring Engineering costs

Legend

KGD	▪ Known Good Dies
Y_{PT} , Y_{WT}	▪ Yield Package Test / Wafer Test
C_{WT} , C_{PT} , C_P	▪ Costs for: Wafer Test / Package Test / Packaging
NRE	▪ Overall NRE Costs

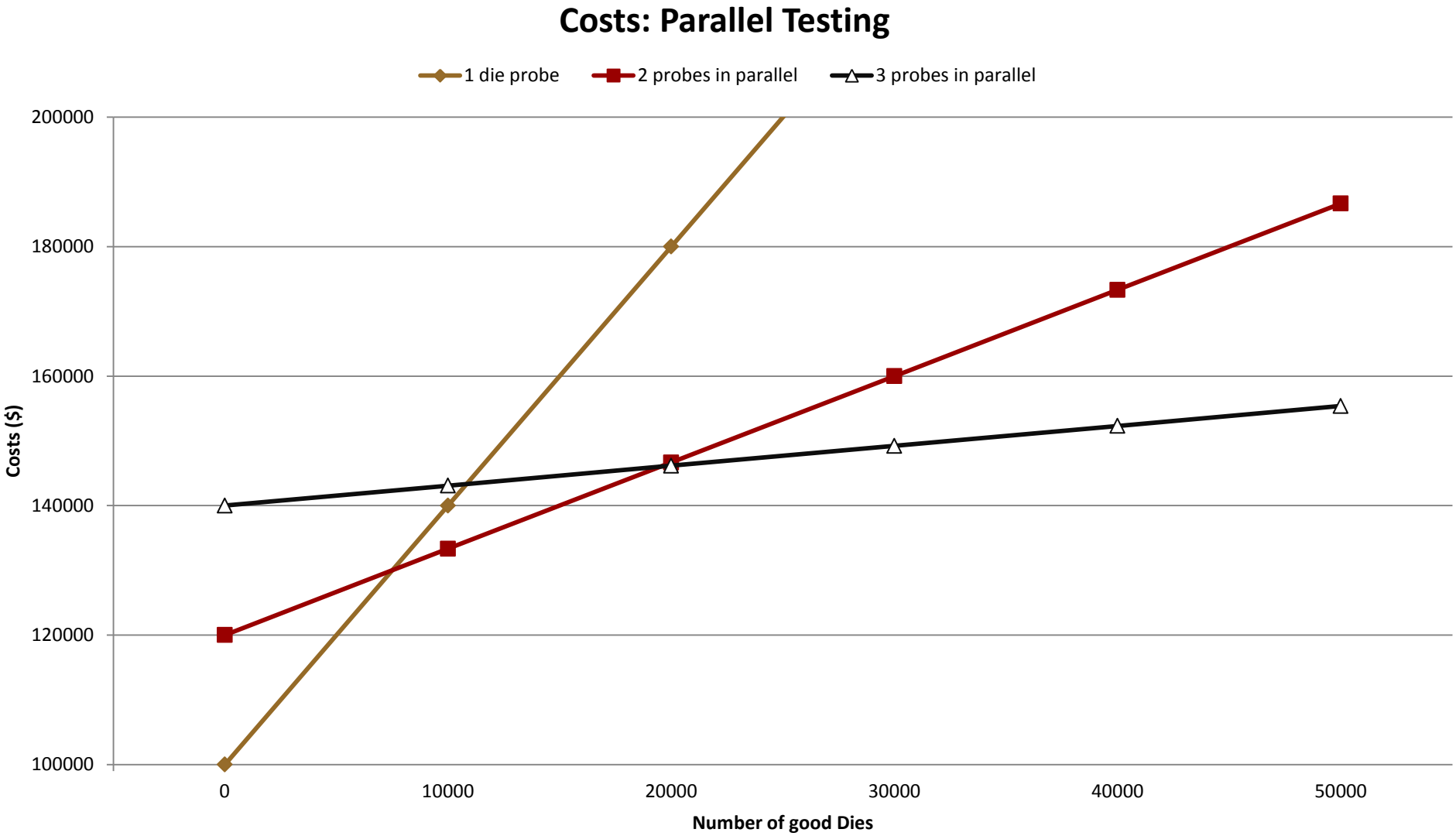
Wafer Level vs. Package Testing: Costs



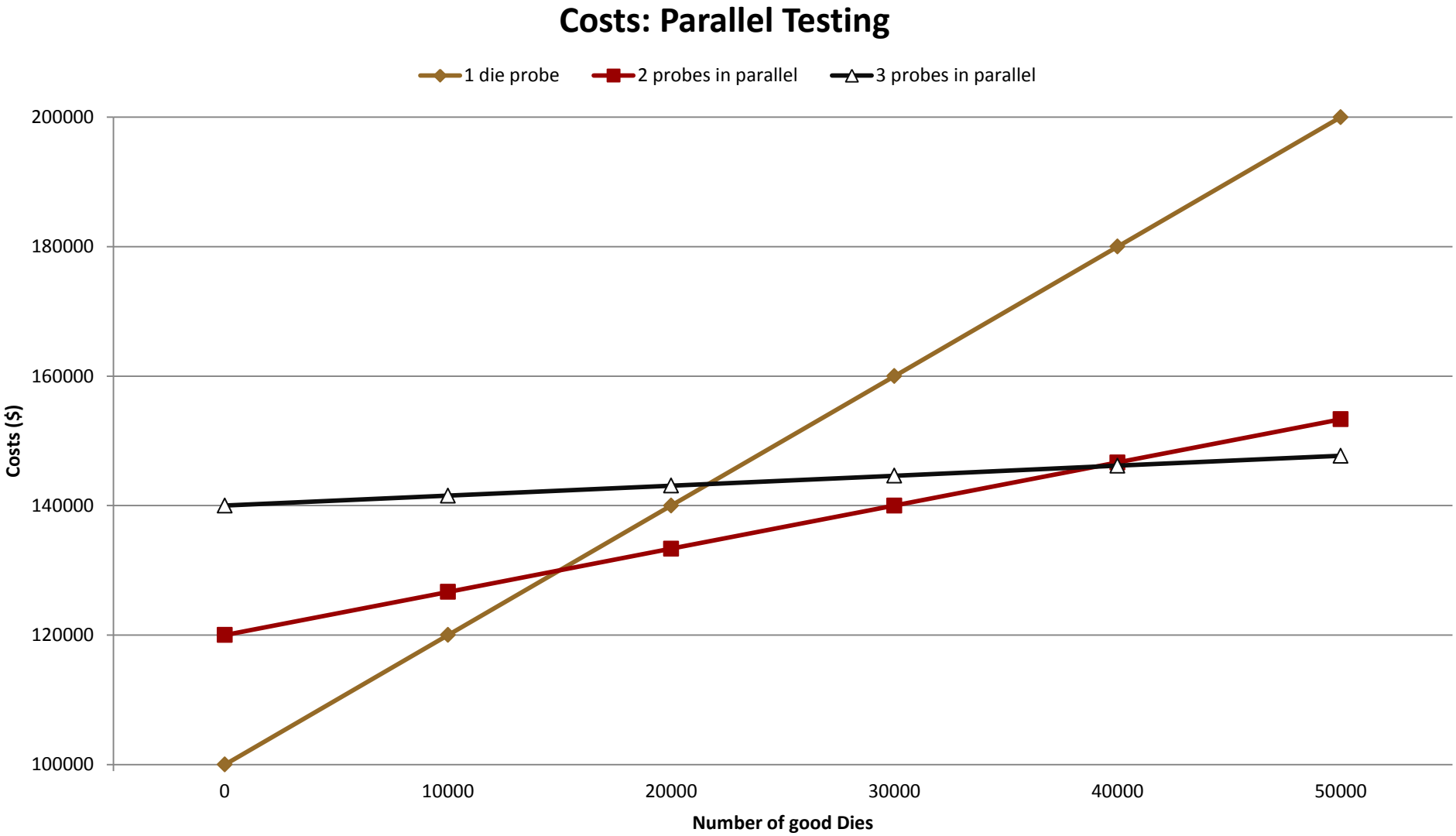
Cost Reduction

- Progress in manufacturing / testing technology
  - New materials
  - New test approaches
    - e.g. Wireless Testing
- Parallel Wafer Level Testing

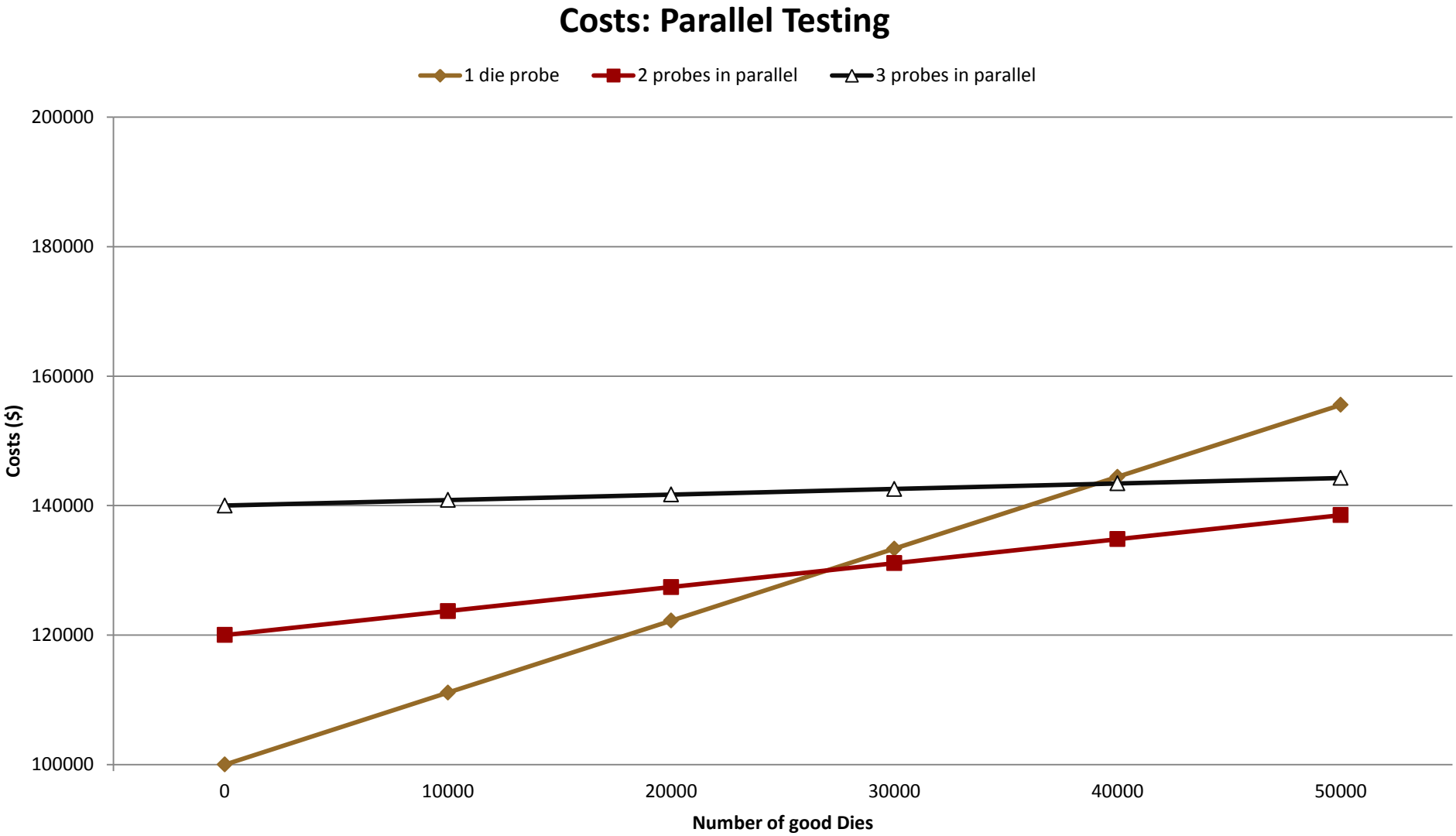
Parallel Wafer Testing: Yield = 0.25



Parallel Wafer Testing: Yield = 0.5



Parallel Wafer Testing: Yield = 0.9



Conclusion

1. Testing is crucial!

2. DFT is crucial!
   - Allows fault detection after manufacturing
   - Importance rises with higher logic density

3. Importance of Wafer Level testing rises with decreasing yield and higher density ICs

4. The best test strategy depends on yield & amount of dies
   - Many parameters. No easy decision !

Outlook

- Future in Wafer Level Testing
  - EMWS: Electromagnetic Wafer Sort by STMicroelectronics

- EMWS:
  - Each die contains tiny antenna
  - Apply test pattern w/o physical contact
  - High power devices still need physical power supply
  - For low-power devices:
    - Power via electromagnetic energy

EMWS[14]

Thank you for your attention !

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