# TSV
# Through Silicon Via Technology for 3D-integration

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***Abstract*—In this paper the Through Silicon Via Technology for 3D-integration will be presented. This technology is an important developing technology that utilises short, vertical electrical connections or "vias" that pass through a silicon wafer in order to establish an electrical connection from the active side to the backside of the die, thus providing the shortest interconnect path and creating an avenue for the ultimate in 3D integration. In the first part of this paper, the steps of the through silicon vias (TSV) technology will be discussed: from the via first approach, a front-end process, to the via last approach, a back-end process. Each of these different ways of elaborating the vias has its advantages and drawbacks. Some Morphological and electrical characterizations of the TSV technology -via shapes, depths, and sizes- will also be showed. In a second part, some applications for TSV in research and industry will be introduced.**

***Keywords— TSV, Via first, Via last, Packaging, DRIE, Silicon etching, Bosch process, FEOL, BEOL, Dry-etching, Wet etching***

## I. Introduction

Through-silicon via (TSV) technology is the heart and most important key enabling technology of three-dimensional (3D) Si integration and 3D integrated circuit (IC) integration. It provides the opportunity for the shortest chip-to-chip interconnects and the smallest pad size and pitch of interconnects. Stacking chips in 3D with TSVs ("Through-Si Vias") as interconnects is today a "hot" new advanced packaging technology platform for memories, CMOS imagers and MEMS. Although the technical challenges for 3D ICs are close to be overcome, the cost of the technology is still a major hurdle. Compared with other interconnection technologies, such as wire bonding, the advantages of TSV include:

1) Better electrical performance
2) Lower power consumption
3) Wider data width and thus bandwidth
4) Higher density
5) Smaller weight
6) Lighter weight
7) Lower cost (hopefully)

There are six key steps in making a TSV:

1) Via formation by either deep reactive-ion etch (DRIE) or laser drilling
2) Dielectric layer deposition by either thermal oxidation for passive interposers or plasma-enhanced chemical vapor deposition (PECVD)
3) Barrier and seed layer deposition by physical vapor deposition (PVD)
4) Cu plating to fill the vias or W (tungsten) sputtering (CVD) for very tiny vias
5) Chemical and mechanical polishing (CMP) of Cu plating residues (overburden)
6) TSV revealing

## II. Who Invented TSV and When

TSV was invented more than 50 years ago by the 1956 Nobel Laureate in Physics, William Shockley. Basically, the "deep pits" (which are called TSVs today) on the wafer allow the signals from its top side to its bottom side and vice versa.

### *A. History of the term "Through-Silicon Via"*

The concept of Through-Silicon Via appeared in late 1990s. The co-founder and current CEO of ALLVIA, Inc. coined the term "through-silicon via" in 1997 as part of his original business plan. From the beginning, the vision of the business plan was to create a through silicon interconnect since these would offer significant performance improvements over wirebonds.[17]

## III. Fabrication Process Overview

3D technologies developed by Yole Developpement consider the 3D IC process steps as a succession of "technological bricks" that can be mixed together: wafer to wafer bonding, chip to wafer bonding, Cu and polySi via filling. All of them depend on the following enabling technologies:

1) TSV formation- realization of electrical isolated connections through the silicon substrate. The diameter of the TSV is dependent on the degree of access needed to an individual strata, which differs with application area.

2) Thinning of the strata-usually to below 50µm in memory stacks, 25 µm for CMOS silicon circuits and to below 5µm for SOI circuits.

3) Alignment and bonding – either as die to wafer or wafer to wafer. Several technologies are available (see fig.1)

In general, the 3 D process sequences discussed in several literature share three common technologies: (1) through silicon via (TSV) formation; (2) IC wafer thinning and (3) aligned wafer od die bonding. Generally, these technologies use reactive ion etching (RIE), chemical vapor deposition (CVD) and chemical mechanical planarization in clean rooms with high cleanness levels. The main attribute of these stacked structures are the z axis interconnects which are usually called "through silicon vias" (TSV) but are also described as "through wafer vias " (TWV) and/ or "through wafer interconnect" (TWI)

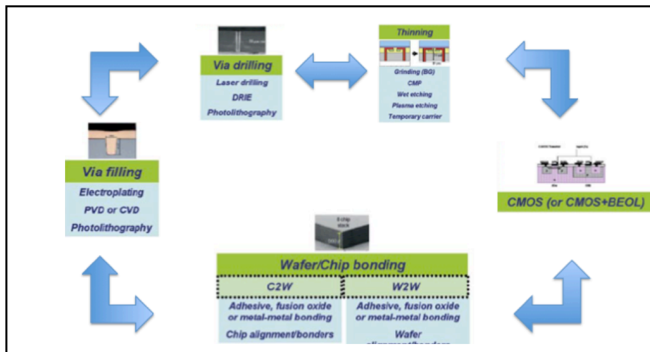



Fig.1: different 3D IC technical steps

## A. *Through Silicon Vias (TSVs) Technology*

TSV (with a new concept that every chip or interposer could have two surfaces with two circuits) is the heart of 3D IC / Si integrations. They are connected to the contact wiring of the devices by standard metallization (aluminium or copper, depending on the technology). (see fig.2 and 3)

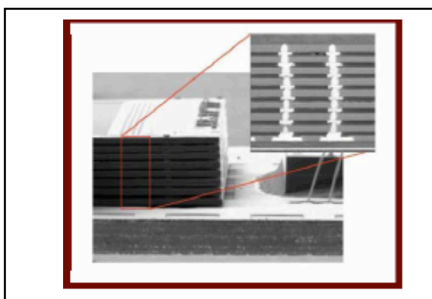


Fig.2: Memory stacks (Samsung) [15]

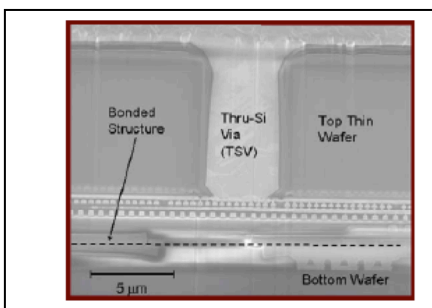



Fig.3: Intel 300 mm multicore processors[15]

TSVs can be categorized by when they are fabricated relative to the IC fabrication process. The major classifications include the following:

1. TSVs fabricated during the IC fabrication process:
a. Front-end-of-line (FEOL) TSVs are fabricated before the IC wiring processes occur.
b. Back-end-of-line (BEOL) TSVs are made at the IC foundry during the metal wiring processes
2. TSVs fabricated following the complete IC fabrication (also referred to as a Post-BEOL TSVs in some books)

## B. *TSV Dimensions*

### 1) *TSV Size today and in the future*

| **Intermediate Level, W2W 3D-stacking** | **2009-1012** | **2013-2015** |
|---|---|---|
| Minimum TSV diameter | 1-2 µm | 0.8- 1.5 µm |
| Minimum TSV pitch | 2-4 µm | 1.6-3.0 µm |
| Minimum TSV depth | 6-10 µm | 6-10 µm |
| Maximum TSV aspect ratio | 5:1 – 10:1 | 10:1 – 20:1 |
| Bonding overlay accuracy | 1.0- 1.5 µm | 0.5 – 1.0 µm |
| Minimum contact pitch | 2-3 µm | 2-3 µm |
| Number of tiers | 2-3 | 8-16 (DRAM) |

Fig.4: TSV Size today and in the future

Figure 4 shows projections from the International Technology Roadmap for Semiconductors. As we can see ,TSV sizes are big today, but it is possible that, minimum TSV sizes will remain in the micron range for the foreseeable future

## C. *FEOL TSVs*

In general, the term front-end-of-line (FEOL) refers to all of the IC process steps preceding the first wiring metal level. The back-end-of-line (BEOL) begins with the first wiring metal level in the IC. It is possible to fabricated TSVs as part of the FEOL process. The conducting material in the FEOL TSV must be doped polysilicon to achieve thermal and material compatibility with the subsequent device processing. These polysilicon TSVs are analogous to deep trench polysicon technology. A major drawback of such FEOL TSVs is the high resistivity of polysilicon compared to metals. However, they can be made conductive enough for many applications and multiple groups are currently developing this technology. CEA

Leti, NEC and Zycube have described processes for FEOL polysilicon TSVs.

### D. BEOL TSVs

BEOL: (Back end of the line ( formation of interconnects in IC fabrication))

The back end of line (BEOL) is the second portion of IC fabrication where the individual devices (transistors, capacitors, resistors, etc.) get interconnected with wiring on the wafer.[1] BEOL generally begins when the first layer of metal is deposited on the wafer. BEOL includes contacts, insulating layers (dielectrics), metal levels, and bonding sites for chip-to-package connections.

TSVs fabricated in the BEOL can consist of either tungsten (W) or copper (Cu). In general the TSV formation occurs early in the BEOL process to insure the TSV will not occupy valuable interconnect routing real estate.

### E. Post-BEOL TSVs

Another option is to fabricate the TSV after the IC fabrication is complete. To fabricate post-BEOL TSVs the ICs must still be specifically designed for 3D integration. For TSVs introduced from the front side of the wafer, an exclusion zone must be present in the IC wiring levels. A major advantage of this approach is that the IC wafers can be of particular importance for applications requiring heterogeneous device technologies (e.g., analog, digital, RF, high voltage, etc.) from various foundries.

### F. "Vias First" and "vias Last"

The Terms "vias first" and "vias last" are used to describe when the TSV fabrication process occurs relative to the other 3D processes of wafer thinning and aligned bonding

## IV. TSV Processes and Integration

### A. Via Creation

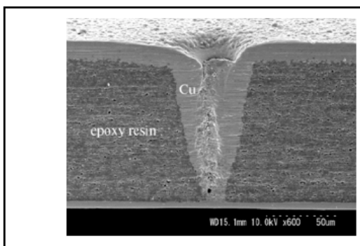



Fig.5: Cross section of Cu plated via [18]

### B. 3D TSV process options

#### 1) Vias

for TSV 3D integration were initially created using laser ablation. However, with the increase in the number of vias and concerns regarding damage and defects, deep reactive ion etch technology, well proven in traditional semiconductor manufacturing, has become the process of choice.
Depending on application, a via first or via last process sequence is followed.

**Via First:** Vias are etched during front-end-of-line processing (i.e., during transistor creation) from the front-side of a full-thickness wafer. This approach is favored by logic suppliers and is the most challenging by far. The smallest via diameters for via-first schemes tend to be 5 to 10µm; aspect ratios are higher (10:1), posing challenges for liner and barrier step coverage, and for the quality of copper fill.

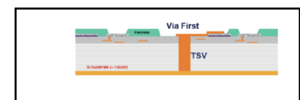



Fig 6: Via First [13]

**In via-first technology**, vias are introduced into the wafers either before device formation (FEOL) or just before BEOL interconnect. In either case, this would occur in the fab prior to completion of the die (wafer).
A key benefit to the via first approach is that companies using it don't need to worry about spoiling expensive wafers at the R&D stage because they can use bare Si or SOI wafers.
One other benefit of the via-first approach is that the TSV brick does not impact the post process flow as the via is fully filled and planarised. Using classic processes like Chemical Mechanical Polishing (CMP) allows finalizing of the TSV brick and results in a planar surface.
Metal–metal bonding is favored by the industry for 3D IC integration because it simultaneously forms both the mechanical and electrical bond. It is also generally accepted that via-first technologies will be significantly easier to manufacture since processing is at wafer scale and the vias are shallower/smaller.

**Via Last:** Vias are etched during or after back-end-of-line processing (i.e., interconnect formation) from the front-side of a full-thickness wafer or backside of a thinned wafer. This approach is used in image sensors and stacked DRAM. CMOS image sensors have via diameters exceeding 40µm with aspect ratios of 2:1. In other devices, the vias range from 10 to 25µm with aspect ratios of 5:1.
The via-last process is usually performed by the fabs with small vias (< 4 µm ) and fine RDLs (<3 µm/ < 3µm

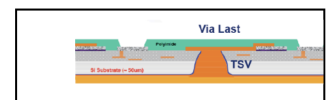



Fig 7: Via Last [13]

*2) Via Fill*

It is very important to choose a suitable material for the TSVs in the 3-D integration technology. Mostly we have employed a low resistive poly-Si for the TSVs since poly-Si is a stable material and affects the device characteristics less than other materials. However, tungsten (W) or copper (Cu) are suitable for the TSV material in the case when TSVs having much lower resistances are required. Specifically, W and Cu are indispensable for scaling down the size of the TSVs.

Experiments have been performed using tungsten and polysilicon as the conductive fill material for TSV vias, especially for the via-first approach. However, both tungsten and polysilicon do not conduct as well as copper and hence copper fill is the mainstream approach today

Via filling includes lining of the deep vias with an inorganic or organic insulator, deposition of a diffusion/ adhesion layer and subsequent conductor fill (Cu, W or pSi). Whether W, Cu, or poly silicon, the vias need to be completely filled, that is, they cannot have voids that would serve to trap processing chemicals.

Beside the formation of TSVs in the front-end process or back-end of line (BEOL), there is also a
post front-end integration process for completely processed and tested CMOS device wafers. Such a process is used in Fraunhofer´s VSI approach. The via filling processes basically deal with chemical vapor deposition (CVD) processes of tungsten or copper or electrochemical deposition (ECD) of copper. Future trends for stacked devices require copper filled TSV for optimized electrical performance. One of the specific characteristics of processes are via dimensions, e.g. via diameter and via depth. The CVD processes is well suited for small sized vias (diameter: 3 µm to 5 µm) with a high aspect ratio (HAR) up to 20 which results in typical via depths in the range of 20 µm to 50 µm. Via sizes larger then 5 µm diameter and via depths acceding 20 µm are preferably filled by a copper electrod eposition process.

*3) Chemical-Mechanical Polishing*

Depending on the TSV processing sequence adopted, chemical-mechanical polishing (CMP) can be used to remove oxide or metal. Challenges include rapid removal of thick materials at low CoO without compromising wafer topography

There are at least two methods to form the TSV. One is by laser drilling and the other by deep reactive-ion etch (DRIE). Laser drilling is a single-point operation, and thus it is cost-effective for small number of vias per chip. DRIE operates on a whole wafer and thus is more suitable for high-density via application. Depending on the kind of laser, the TSV hole size and pitch are limited for a CO2 laser, via hole size = 65 µm (top) and 25 µm (bottom), pitch = 125 µm; and for Excimer laser, via hole size = 18 µm (top) and 12 µm(bottom), pitch = 35 µm].

On the other hand, with DRIE, the TSV hole size and pitch can go down to as small as 1 and 5 µm, respectively. Most potential applications of TSV are in the range of 5 µm <= TSV hole size <= 20 µm and 20 µm <= pitch.

## V. Via Forming

### A. *DRIE Bosch technology (Dry-etching)*

In the mid-1990s Deep Reactive Ion Etching (DRIE) was introduced by Bosch and commercialized by several equipment manufacturers.
The Deep Reactive Ion Etching (DRIE) Bosch etch process is used close to its best capability to achieve such very deep structures. Bosch etch process on Deep Reactive Ion Etching (DRIE) is commonly used for years.

**(DRIE)** is by far the most commonly used technology to form the TSV hole due to its excellent process controllability and its capability to create high aspect ratio via (up to 110:1) and adopted sidewall profiles and topographies.

The generic process flow by via forming is briefly described:

First, the high aspect ratio via are formed by RIE Fig.8: using a so called Bosch-Process with a photo resist mask.

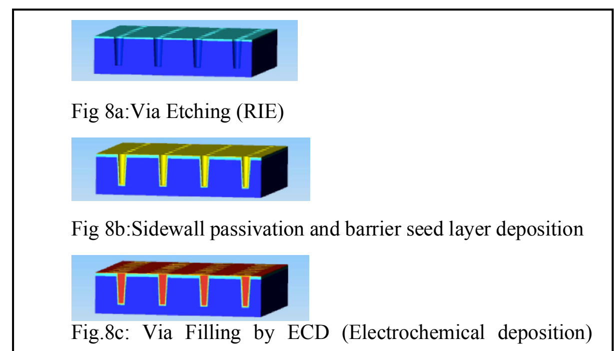


Fig 8a:Via Etching (RIE)

Fig 8b:Sidewall passivation and barrier seed layer deposition

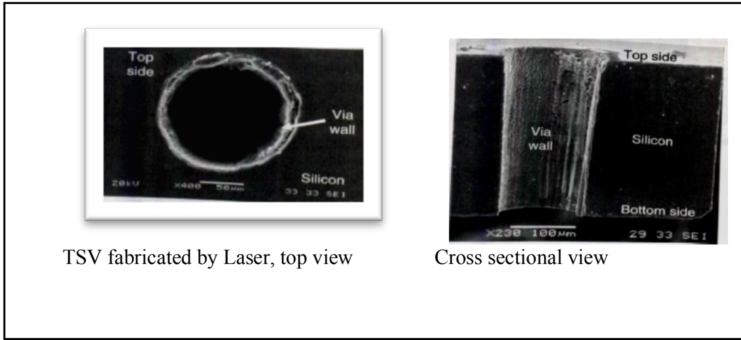
Fig.8c: Via Filling by ECD (Electrochemical deposition)

Figure 8a-c: Generic process flow for silicon interposer with Through Silicon Vias [21]

### B. *Laser Driling technology (Wet-etching)*

Laser drilling is a single-point operation, and thus it is cost-effective for small number of vias per chip.

Also, it should be pointed out that the surface condition of the laser drilled vias is very rough, as shown in Figure 9:




TSV fabricated by Laser, top view Cross sectional view

Fig. 9: TSV fabricated by Laser, top & Cross sectional view [2]

The roughness is obvious. Some chemical polishing is needed to obtain a smooth wall, which increases the manufacturing steps and cost

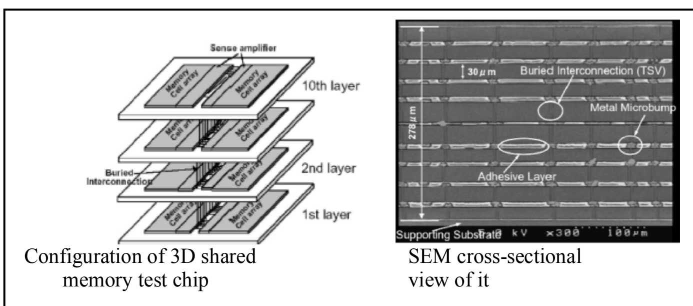
Based on the literatures, more than 95 percent of vias habe been formed by DRIE Bosch technology, which is a highly anisotropic etching process. The silicon vias can be formed in an inductive-coupled plasma (ICP)-based DRIE system such as that from Applied Materials and SPTS. (SPTS) means SPP Process Technology Systems, a subsidiary of Sumitomo Precision Products ('SPP') and leading manufacturer of etch, deposition, and thermal processing equipment for the semiconductor industry.

Although the ICP system is designed mainly for performing deep reactive-ion etching of silicon by a specially designed switched etch and passivation process, also known as the Bosch Process, it can be used in reactive-ion etch mode, referred as the non-Bosch process. [2]

## VI. Applicability

### *A. 3-D shared memory test chip with ten memory layers*

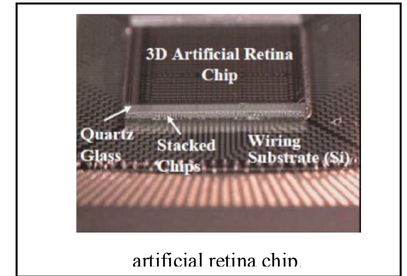
3D integration is a reality today with several foundries offering 3D packaging and Through-Silicon Via (TSV) technology.




Configuration of 3D shared memory test chip SEM cross-sectional view of it

Fig.10: 3D shared memory [4]

### *B. 3-D artificial retina chip*



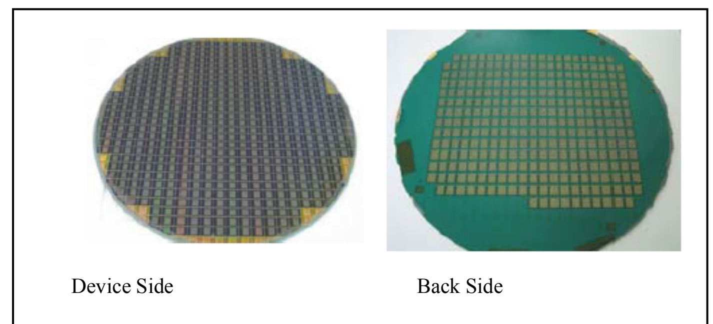

artificial retina chip

Fig.11: 3D artificial retina chip [26]

This artificial retina chip has a three-layer structure. Functions of the horizontal cell layer, bipolar cell layer, amacrine cell layer, and ganglion cell layer are simplified and allocated into two layers of an artificial retina chip. A quartz glass is glued on top of this artificial retina chip.

### *C. CMOS image sensor package / TSV CMOS Image Sensor (TSV CIS)*

One of the first applications to make use of 3D stacking/ TSV will be CMOS image sensor chips for cell phones. CMOS sensing chips must mount face up. Minimal package device size is obtained by creating TSV and connecting directly to the backside of the chip. The obvious solution of having the active area of the sensor face up and the interconnect on the backside of the device is easily obtained by backside formation of TSV. The backside illumination technique has significant advantages over the front-side illumination due to separation of the optical path from the metal interconnects. Wafer bonding plays a key role in manufacturing backside illuminated sensors. Tessera, Schott Glass, Fujikura, Sanyo, Toshiba, Zycube and others are developing and commercializing such TSV "packages."[1]



Device Side Back Side

Fig12: Wafer-level package of CMOS image sensor [24]

## VII. Conclusion

### A. Yield Issue

The yield of 3D integration is the most controversial discussion within the industry. Stacking of dies has the inherent risk that if one layer is defective the whole device is defective.

### B. Resumee

Although the technical challenges for 3D ICs are close to be overcome, the cost of the technology is still a major hurdle. TSVs have many advantages: smaller form factor, better performance … but they also have to face many competing stacking technologies (PoP, PiP) for which competing interconnect technology such as wire bonding is very low cost.

Using polySi (when it is possible) is less costly than using Cu for via filling and this approach is likely to be used for DRAMs. Via etching is not the most expensive process step. Bonding and filling account for the major part of a TSV process final cost.

For Silex, Bauer says the biggest technical challenge is to achieve a working solution for the fundamental problem of thermal coefficient of expansion (CTE) mismatch between metals and the commonly used wafer substrate materials.

To conclude this paper, key features characterizing this through silicon via process are listed below:

1. High density via technology (pitch <50 μm)
2. ”No metal” starting material with unrestricted MEMS or CMOS post processing capability
3. Enables true wafer level packaging of MEMS devices with vacuum sealing
4. Low cost solution due to minimized component form factor and ”all silicon package” for SMD assembly
5. First through wafer via technology in volume production

Finally we would like to point out that, the exact design of the via and the fabrication process flow depends very much on the application, i.e. the via integration concept.

## VIII. Abbreviations and Definitions

**CTE** thermal coefficient of expansion

**SEM** scanning electron microscope

**PIP** Package-Interposer-Package

**PoP** Package-on-Package

**RDL** Redistribution layer

**CoO** Cost -of -Ownership

**VSI** Vertical System Integration

**Via First** building through-silicon vias into the wafer before bonding

**Via Last** creating through-silicon vias after wafers have been bonded

**MEMS** Microelectromechanical system

**DRIE** deep reactive-ion etch

**FEOL** Front End Of Line: any process performed before the metal interconnect is laid down

**BEOL** Back End Of Line: any process performed during the creation of metal Interconnect

**TSV** Through-Silicon Via: a vertical interconnect piercing the body of a die in a 3 D IC

**CVD** Chemical Vapour Deposition

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