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„Through Silicon Via for 3D integration“

Myth or reality ?

Advanced Seminar „Computer Engineering“
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Outline

1) Basic Definitions

2) 3D IC process flow with the different steps

3) TSV Process fabrication

4) Summary and Discussion

3D BACKGROUND TECHNOLOGY

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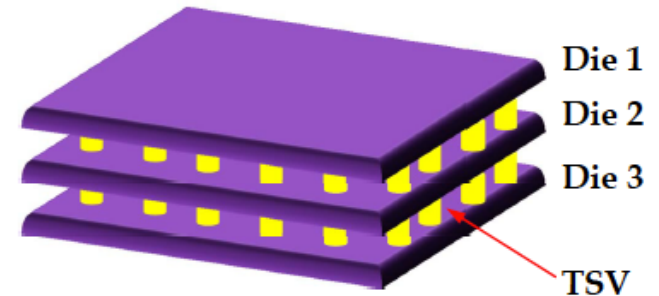
Some Basic Definitions

- **TSV**

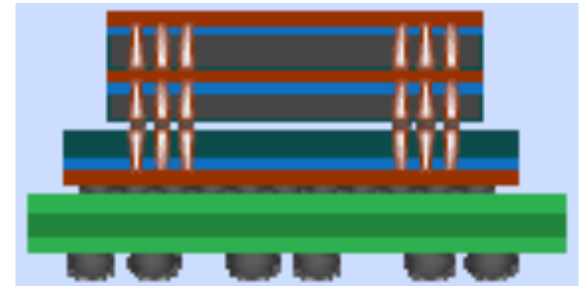
Through Silicon Via. A via that goes through the silicon substrate that enables connection from top to bottom



[2] http://www.ee.ncu.edu.tw/~jfli/vlsi2/lecture/ch07.pdf

- **3D-IC**

Multiple dies are stacked and TSV is used for the inter-die interconnection



[3] http://asia.stanford.edu/events/Spring05/slides/051205-Koyanagi.pdf

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Some Basic Definitions

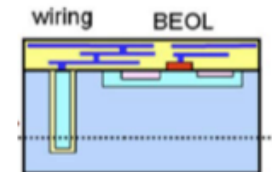
- **FEOL TSV**

  Front-end-of-line TSVs are fabricated before the IC wiring processes occur.

[4]http://jsa.ece.uiuc.edu/tsv/Yokohama_paper.pdf

- **BEOL TSV**

  Back-end-of-line (BEOL) TSVs are made at the IC foundry during the metal wiring processes

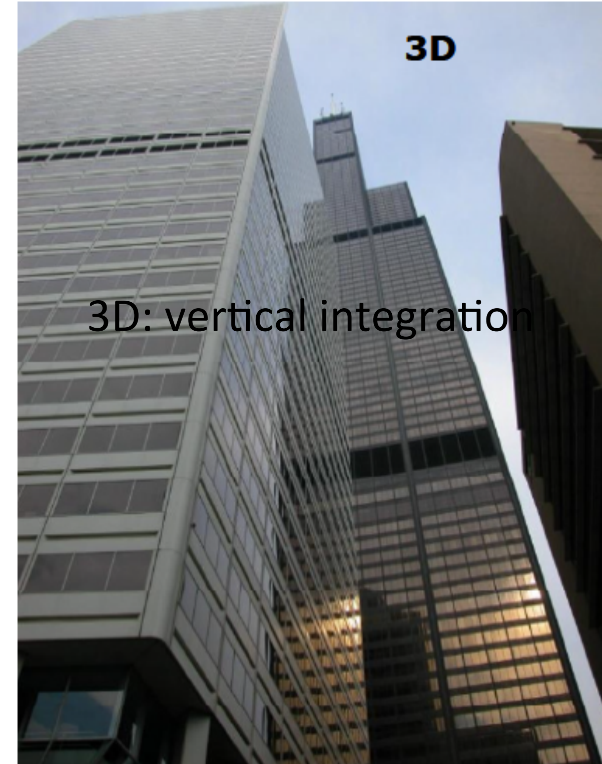


[5]http://jsa.ece.uiuc.edu/tsv/Yokohama_paper.pdf

3D Real estate analogy

2D: Side-by-side placement (horizontal)

[6] http://www.aspdac.com/aspdac2009/archive/pdf/4D-1.pdf



[7] http://www.aspdac.com/aspdac2009/archive/pdf/4D-1.pdf

3D IC PROCESS FLOW WITH THE DIFFERENT STEPS

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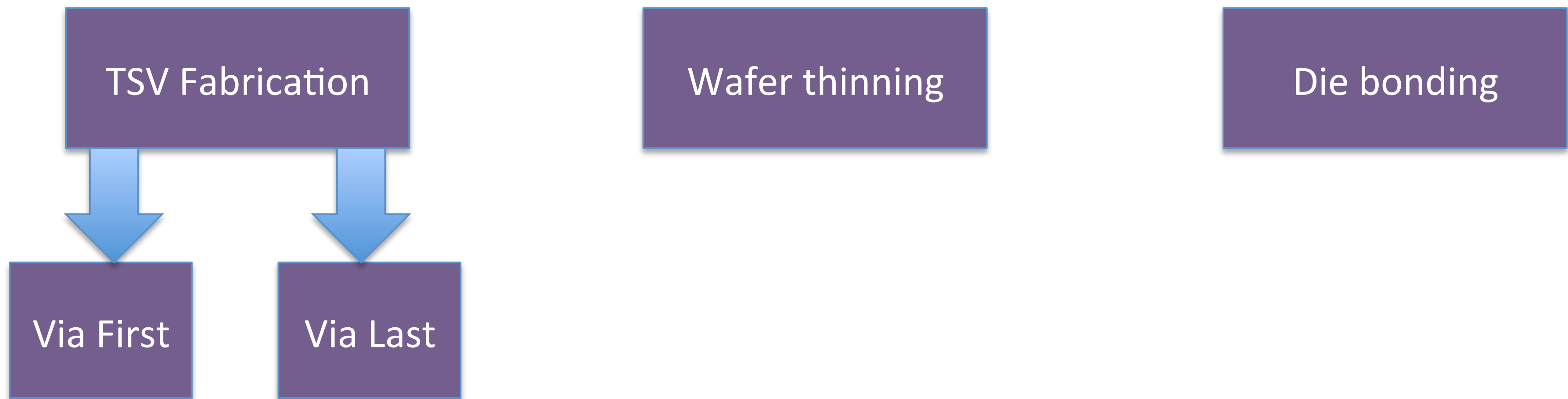
3D IC process variations

- Three majors process technologies:



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TSV fabrication process variations.

- TSVs can be categorized by when they are fabricated relative to the IC fabrication process.

No TSV	Via First	Via First „FEOL“	Via First „BEOL“	Via Last „copper liner“
	TSV			
„FEOL“				
		TSV		
„BEOL“				
			TSV	
„Thinning“				
„Bonding“				
				TSV

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Animation (technology steps)

- A short animation for the chip-level 3D integration process, illustrated the technology steps:

TSV PROCESS FABRICATION

TSV Processing

Via formation

-Deep reactive-ion etching

-Laser

-Other (e.g. wet chemical etch)

+ Via Filling

Material: Copper, Tungsten, polysilicon

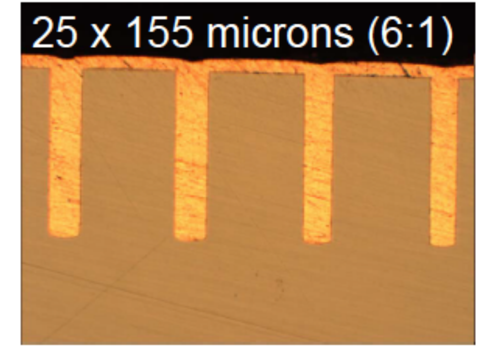
Different Materials require different deposition processes (electroplating, CVD, LPCVD)

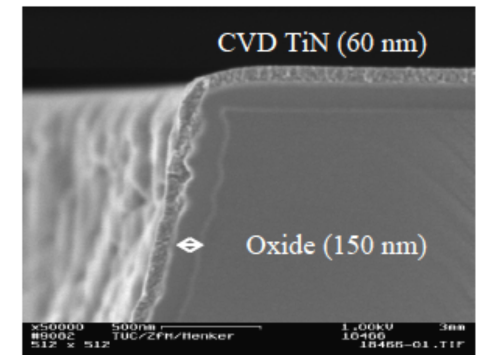
Cu is the most widely used material today

Wafer Stacking

Cu diffusion, adhesive or fusion bonding

Micro-bumping





[8]M. Young, The Technical Writer’s Handbook. Mill Valley, CA: University Science, 1989.

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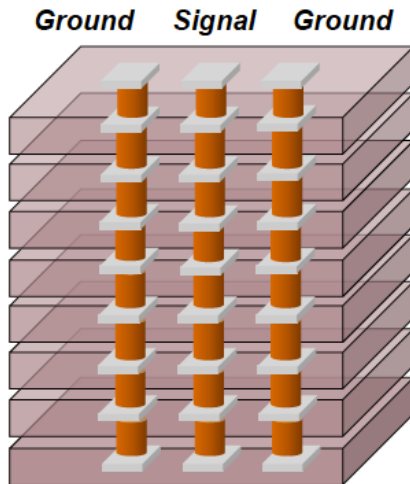
TSV(Typical Design Values)



[9]M. Young, The Technical Writer's Handbook. Mill Valley, CA: University Science, 1989.

TSV dimension

TSV diameter	**75 µm**
TSV height	90 µm
TSV-to-TSV pitch	150 µm
SiO_2 thickness	0.1 µm
Number of stacked dies	8

Ohmic Contact information

Junction depth	**1 µm**
Resistivity of Silicon	10 Ω.cm
Contact Width	22.5 µm

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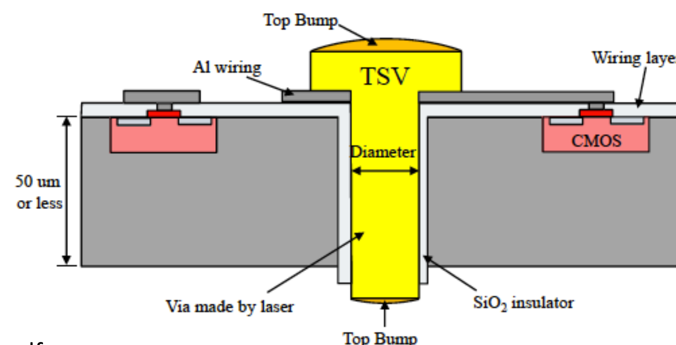
TSV Size Today and in the future

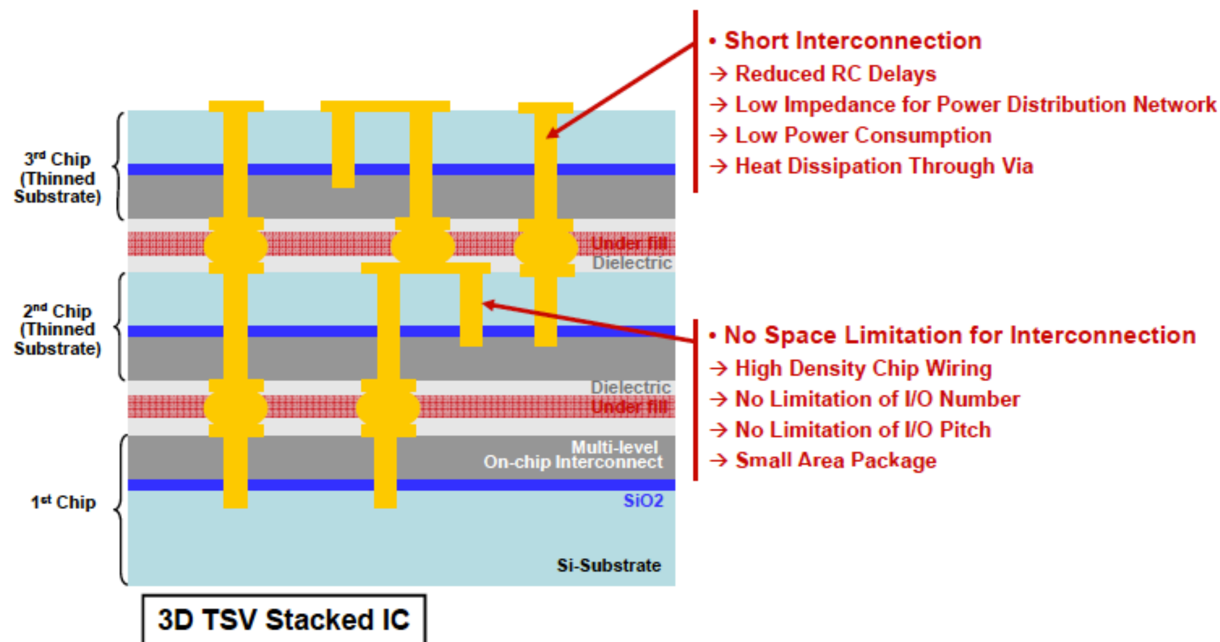
Intermediate Level, W2W 3D-stacking	2009-1012	2013-2015
Minimum TSV diameter	1-2 µm	0.8- 1.5 µm
Minimum TSV pitch	2-4 µm	1.6-3.0 µm
Minimum TSV depth	6-10 µm	6-10 µm
Maximum TSV aspect ratio	5:1 – 10:1	10:1 – 20:1
Bonding overlay accuracy	1.0- 1.5 µm	0.5 – 1.0 µm
Minimum contact pitch	2-3 µm	2-3 µm
Number of tiers	2-3	8-16 (DRAM)



[11] http://www.ee.ncu.edu.tw/~jfli/vlsi2/lecture/ch07.pdf

TSV Barrier

- TSV Isolation Liner Process: In order to electrically isolate the TSV connections from the SI substrate, an isolation layer is required
- Prevalent barrier materials used are Ta and TiN



[13]http://www.sematech.org/meetings/archives/3d/8334/pres/Fukushima.pdf

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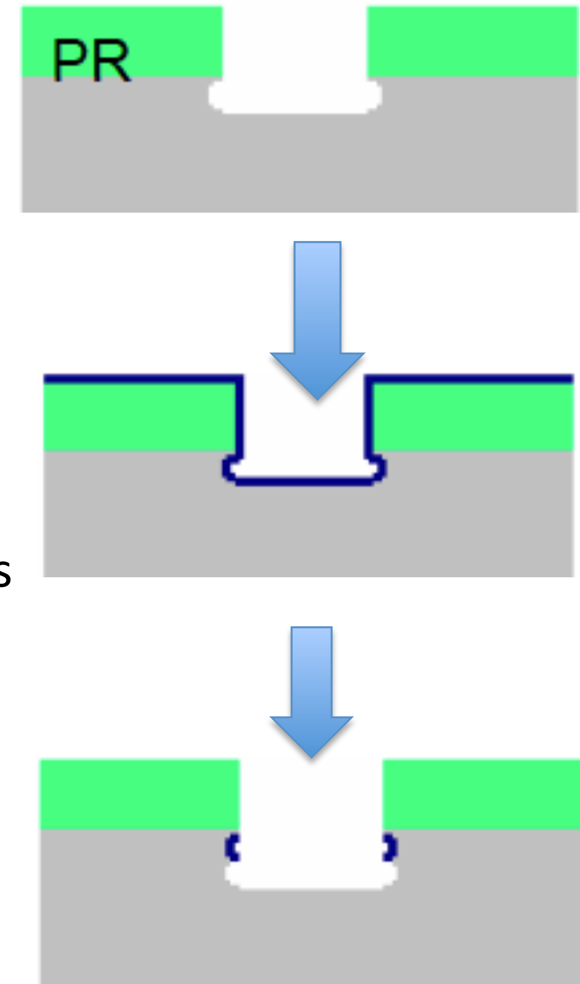
VIA FORMATION METHODE

DRIE Method (Bosch Process)



- Deep reactive-ion etch (DRIE)
- Where passivation and etching steps are alternating in time

  - allows for high aspect ration etching

  DRIE : AR ◊ 17 to 33

  Etch depths (30-100 µm)

- The prevalent technique used is the ´Bosch´ Process

Bosch Process advantages

- Can be conducted at room temperature
- Low temperature sensitivity

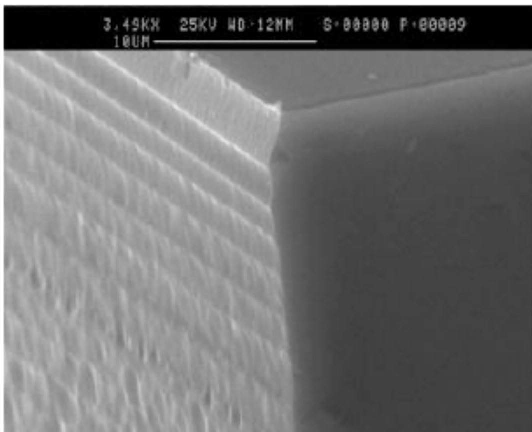
DRIE vs Laser Drilling

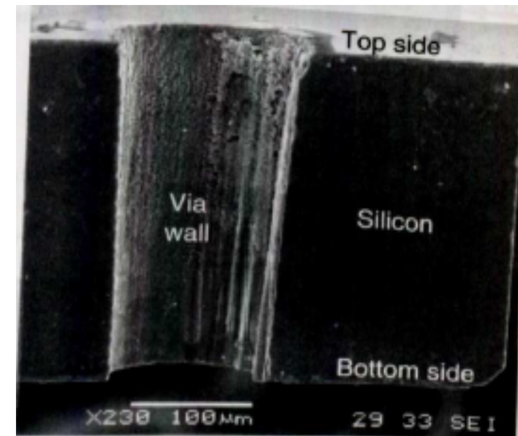
Deep reactive-ion etch (DRIE)
DRIE Bosch Method

highly anisotropic etch process used to create deep penetration
Based on the literatures >95 % vias

Laser Drilling Method

Single-point operation
a process in which a laser is used to make holes, instead of conventional drilling.





[14]http://asia.stanford.edu/events/Spring05/slides/051205-Koyanagi.pdf

[15]http://asia.stanford.edu/events/Spring05/slides/051205-Koyanagi.pdf

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TSV Processes

- 3D Integration Processes, Methods, and Options

Processes	Methods/Options	
Via forming	**Bosch DRIE**	**Laser**
Dielectric deposition	SiO2	Polymer
Barrier/seed layers deposition	Ti (or Ta)/ Cu	W/W
Via filling	Cu	Conductive polymer, CNT, solder, etc.
TSV revealing	Wet etch	
TSV process	TSV before bonding, TSV after bonding	Via last (front-or back-side)
Stacking	C2C	W2W
Micro interconnect	Solder bump	

[12]http://iopscience.iop.org/1748-0221/4/03/P03009/pdf/1748-0221_4_03_P03009.pdf

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VIA FIRST

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TSV for bonding

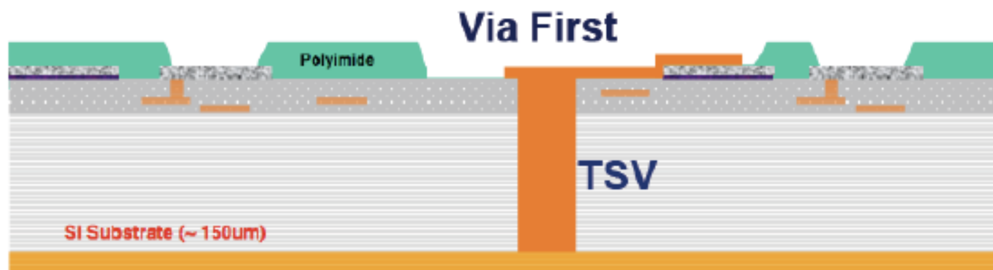
VIA-FIRST

- Vias created early in the device manufacturing process
- Issues with temperature compatibility of subsequent CMOS steps
- Materials must be CMOS compatible

  Targetresistance: < 1 Ω

  Only known good wafers are used

  Lower cost than via-last



[16]Image Courtesy of Amkor

VIA LAST

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Via after Bonding

- No thermal stress issues
- Via location must be considered during design phase
- Large via feature (Ø up to bond pad size),
- low via density via pitch ~100-150µm
  - – Wafer thickness <200µm

-via area has to be reserved designing the chip
-area for vias introduces dead area in CMOS chip
complicated process flow

[17]Image Courtesy of Amkor

Video (3D IC Process description)

Source: Projektgruppe ASSID (All Silicon System Integration Dresden) des Fraunhofer IZM.

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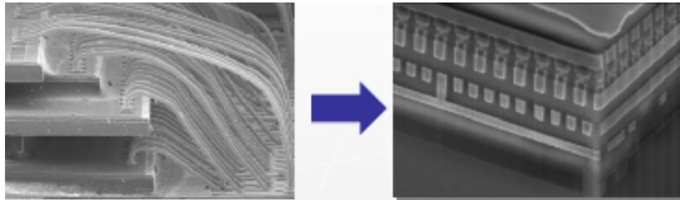
3D Integration Drivers

+ **Image sensors** and **memory stacking** (for mobile applications) are two mass volume applications for TSVs with short time-to-market

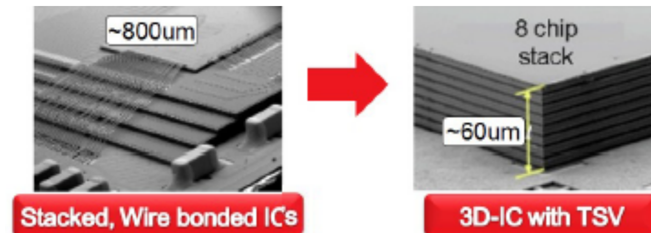
These are all potential 3D drivers:

[18]14. L. Bernstein, H. Bartolomew, Trans. Met. Soc. AIME **236**, 404 (1966).

3D-IC Advantages



[19]http://www.sematech.org/meetings/archives/3d/8334/pres/Fukushima.pdf



[20]http://www.sematech.org/meetings/archives/3d/8334/pres/Fukushima.pdf

- ✓ Performance:
  - Higher bandwidth
  - Shorter wire length
  - Shorter critical paths
- ✓ Lower Power
  - Reduced wire L and C
  - Shorter interconnect paths
- ✓ Mixed die technologies
  - Heterogeneous technologies
  - Mixed technology generations
- ✓ Smaller form factor
  - Reduced area and thickness

TSV APPLICABILITY

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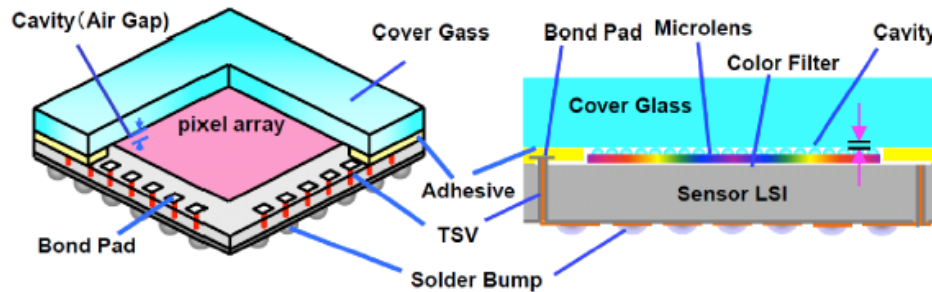
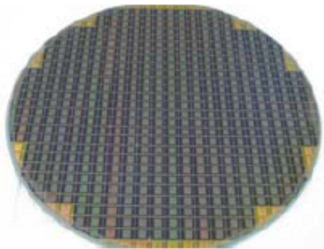
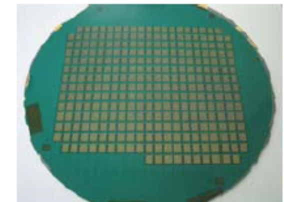
CMOS image sensor package



The schematic diagram of a CSP for image sensors. TSVs connect the bond pad and the backside bump.

[21]http://iopscience.iop.org/1748-0221/4/03/P03009/pdf/1748-0221_4_03_P03009.pdf





Back Side

Device Side

Wafer-level package of CMOS image sensor

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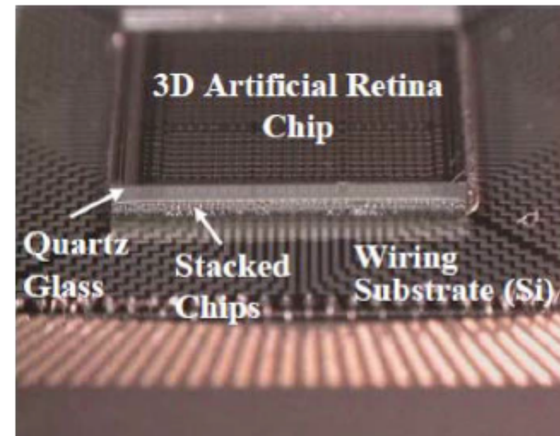
3-D artificial retina chip

1) Reception cell
2) Retina cell
3) Bipolar cell
4) Amacrine cell
5) Ganglion cell



Photomicrograph of 3-D artificial retina chip.

[22]http://www.sematech.org/meetings/archives/3d/8334/pres/Fukushima.pdf

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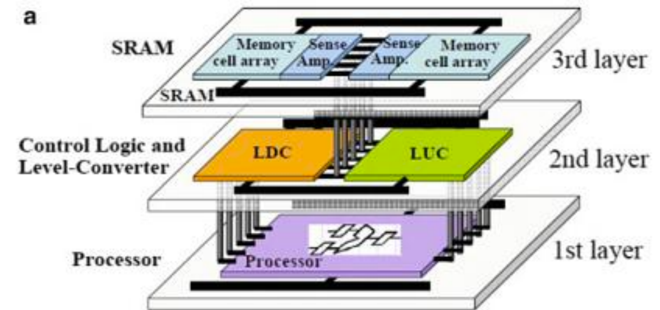
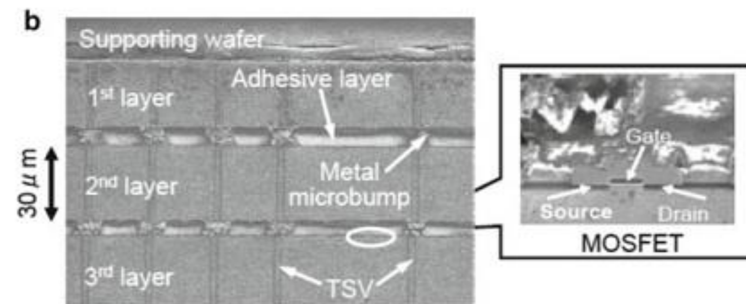
3D µprocessor Chip

- ✓ CPUs are connected to the respective memory layers of the 3D shared memory



- ✓ 14x increase in memory density
- ✓ 4x Logic Cost Reduction
- ✓ $29^x \rightarrow 100^x$ memory cost reduction



[23]http://www.sematech.org/meetings/archives/3d/8334/pres/Fukushima.pdf

CONCLUSIONS, AND FUTURE PROJECTIONS

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Conclusion

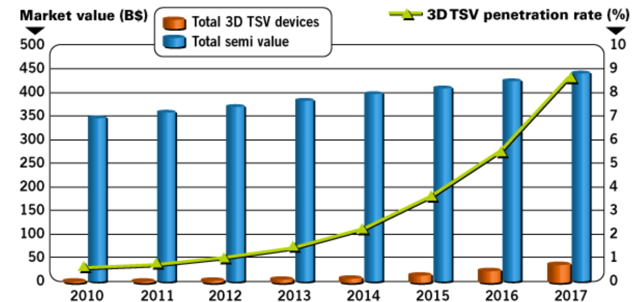
- 3D TSV packages outgrow semiconductor industry by 10X.

Cost Analysis for 3D Integration with TSV

- Although the technical challenges for 3D ICs are close to be overcome, the cost of the technology is still a major hurdle.

Annealing

- The greatest technological challenge is heat control

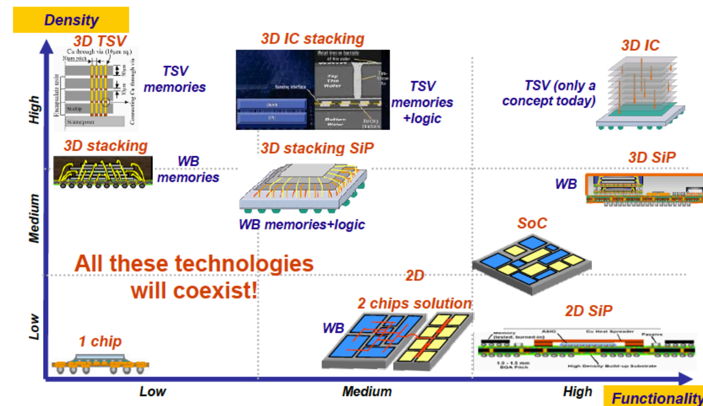


[24]http://www.aspdac.com/aspdac2009/archive/pdf/4D-1.pdf

Future Projections

The bottom line is:

3D through silicon via (TSV) chips will represent 9% of the total semiconductors value in 2017



[25]http://www.csmantech.org/Digests/2007/2007%20Papers/02d.pdf

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Thank you for your attention

Questions?

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[2] http://ecadigitallibrary.com/pdf/58thECTC/s13p5p43.pdf

[3] http://jsa.ece.uiuc.edu/tsv/High_density_Paper.pdf

[4] http://en.wikipedia.org/wiki/Through-silicon_via

[5] http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=4550029

[6] http://www.ae.utexas.edu/~ruihuang/talks/TSV_April2010.pdf

[7] P.Garrou, „wafer Level 3D integration,“ presented at peaks in packaging Whitefish Montana, Sept. 5-7, 2007

[8] P. Garrou and C. Bower, "Overview of 3D Integration Process Technology", Chapter 3 in Handbook of 3D IC Integration: Technology and Applications, P. Garrou, C. Bower and P. Ramm Eds. , Wiley VCH, 2008

[9] P. Enquist, "3D Integration at Ziptronix", chapter 25 in Handbook of 3D IC Integration: Technology and Applications, P. Garrou, C. Bower and P. Ramm Eds., Wiley VCH, 2008.