Current Trends in Hybrid FPGA/CPU Devices

Xilinx Zynq Series – Real Innovation or Temporary Hype?

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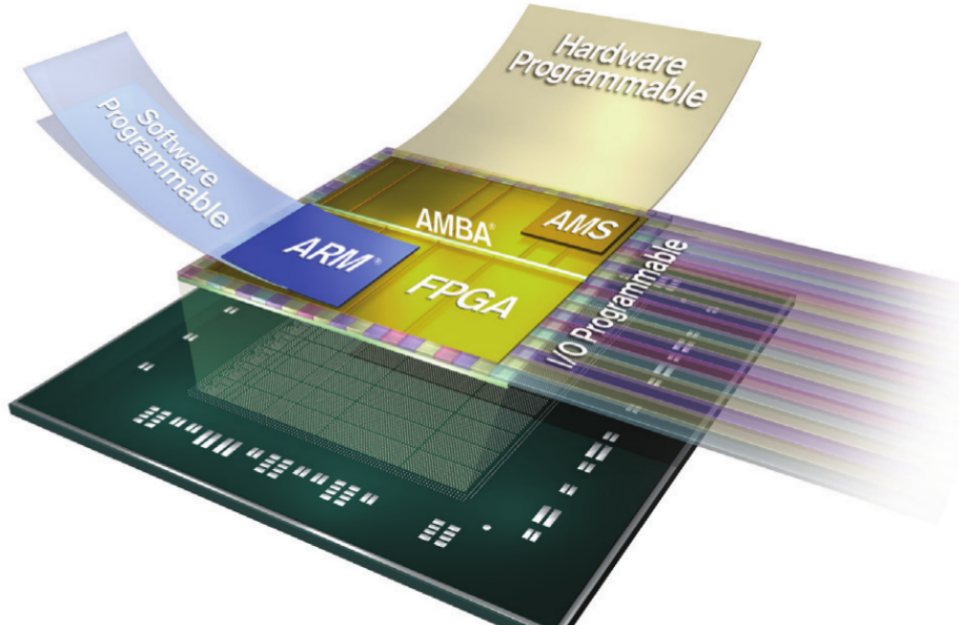
5th February, 2014



Agenda

Embedded Systems

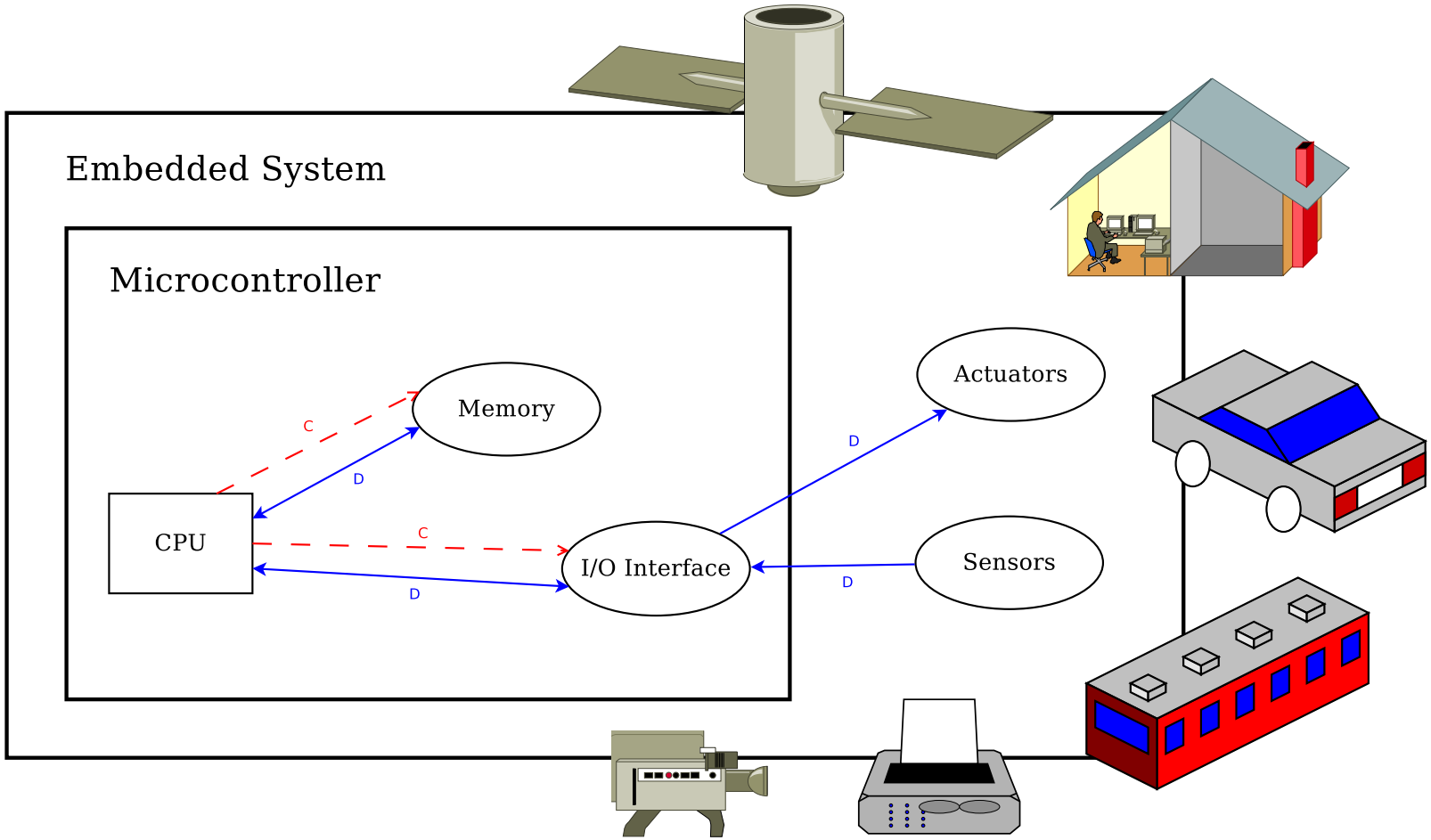


Figure 1: Relation of Embedded Systems and Microcontrollers

[1–4]

FPGAs

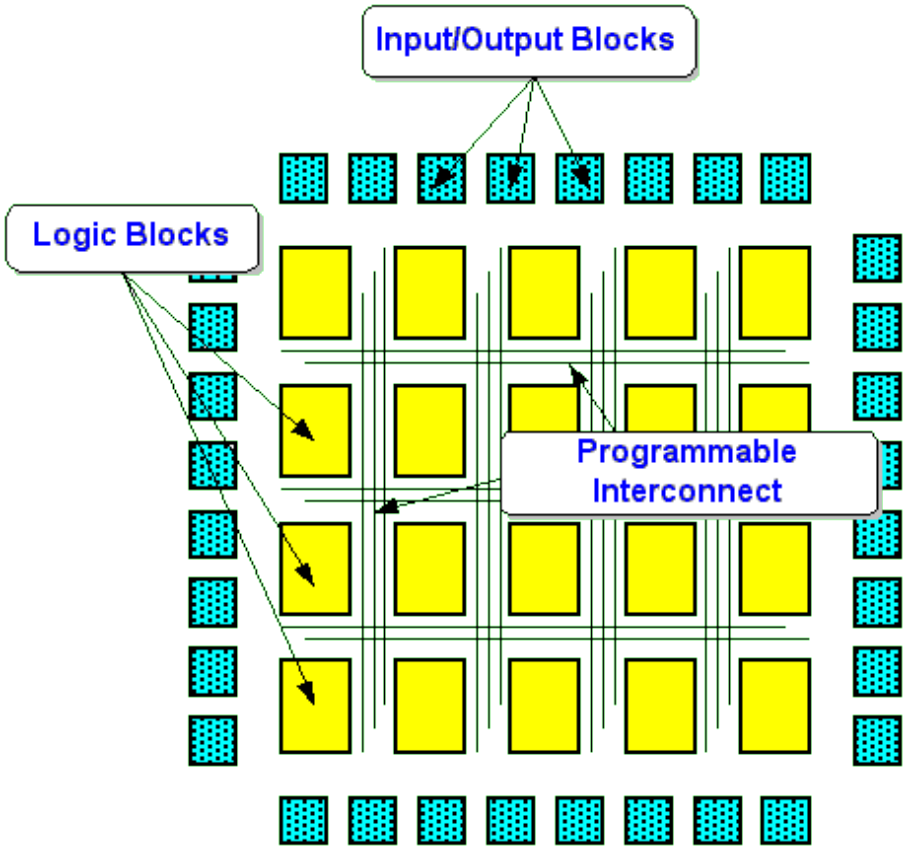


Figure 2: FPGA Structure [5]

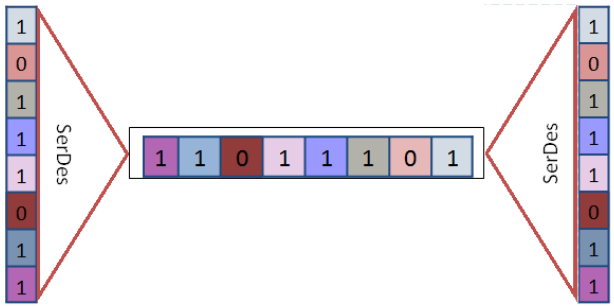


Figure 3: Functionality of a SerDes [6]

[1, 2, 7–10]

FPGA Design Flow

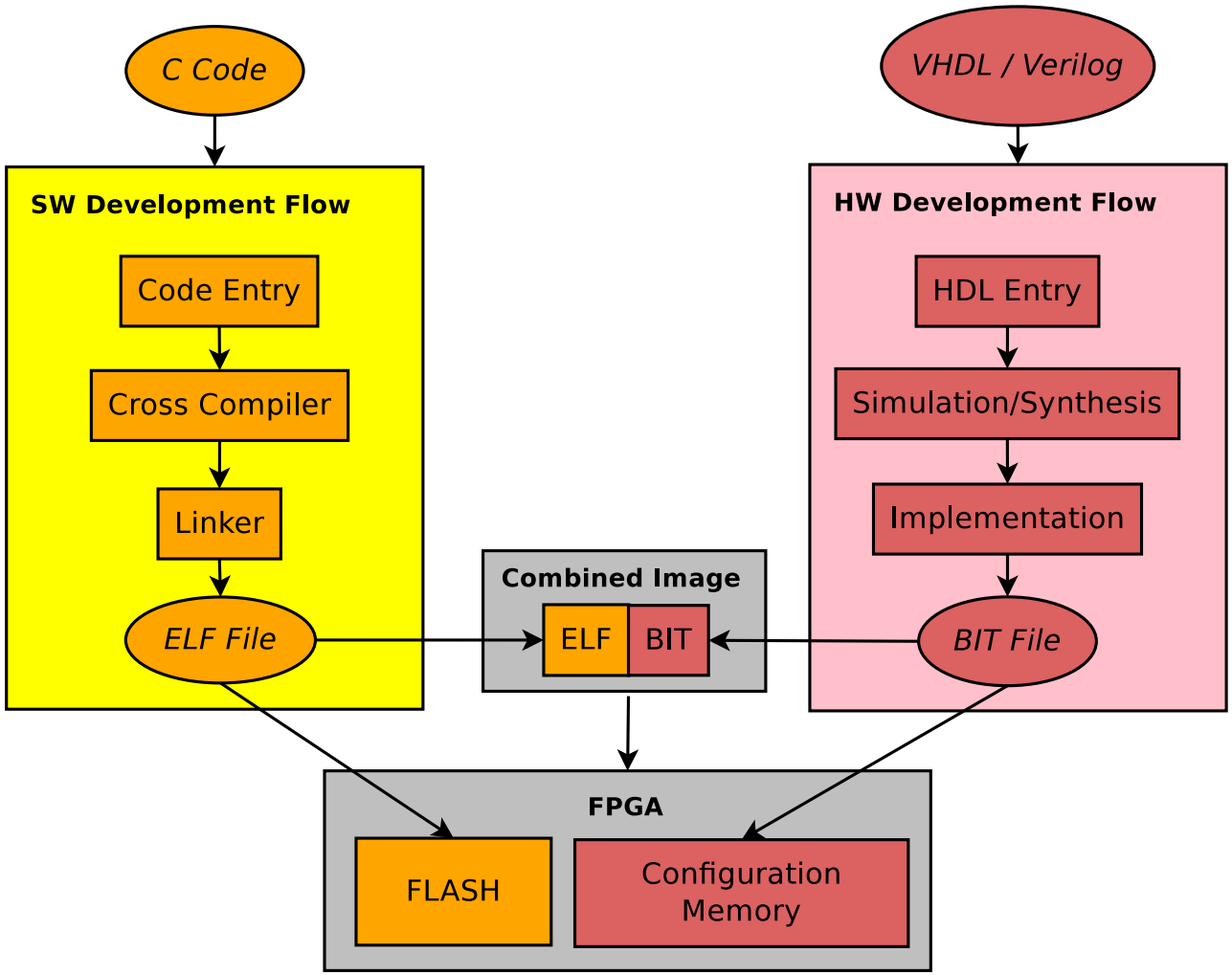


Figure 4: Xilinx' FPGA Design Flow (simplified) [based on 9, slide 8]

[1, 2, 7–10]

FPGA Embedded Processors

Fixed Hardware

- Discrete Processor

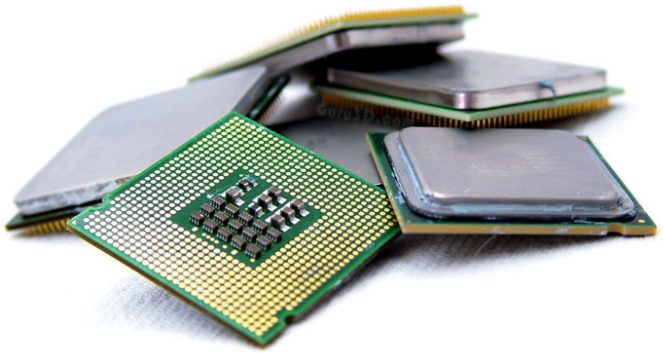


Figure 5: Discrete Processors [11]

Reconfigurable Hardware

- FPGA
- Hybrid

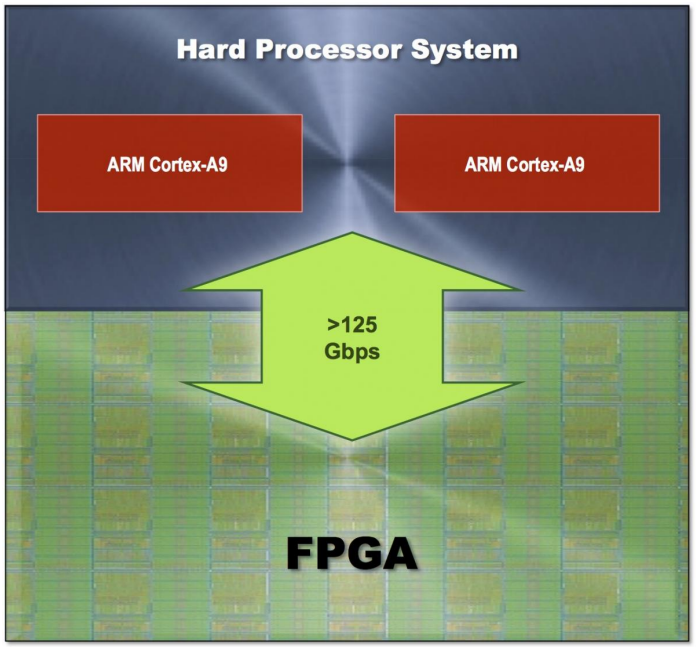


Figure 6: Altera's Idea of Hybrid Devices: "Hard" CPU Plus FPGA [12]

[1, 2, 7–10]

Architecture

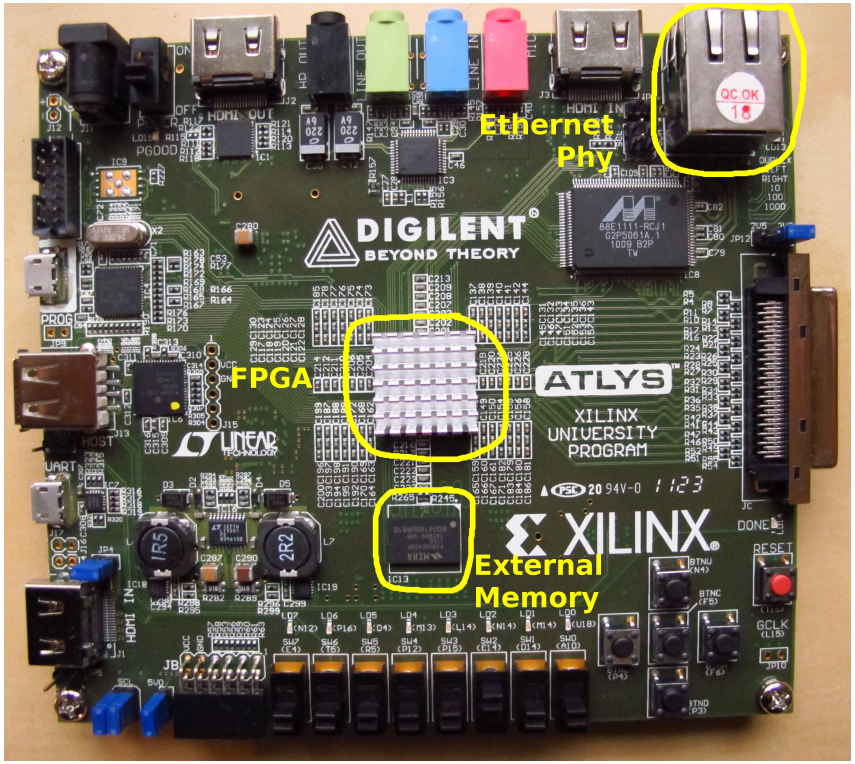


Figure 7: Atlys Spartan-6 FPGA Development Board

[7, 8]

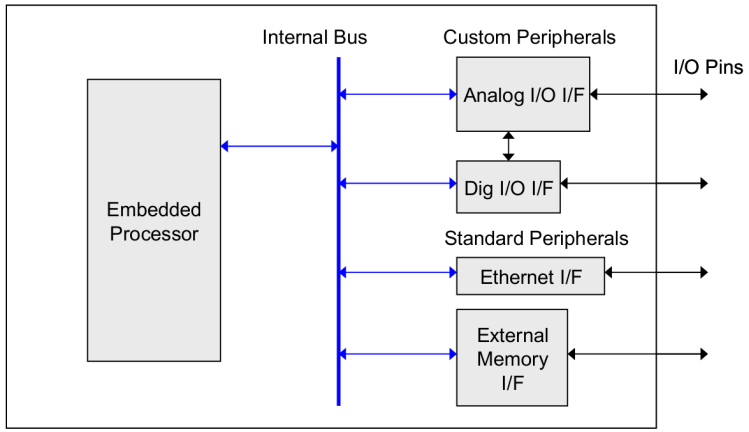


Figure 8: FPGA with Embedded Processor [7]

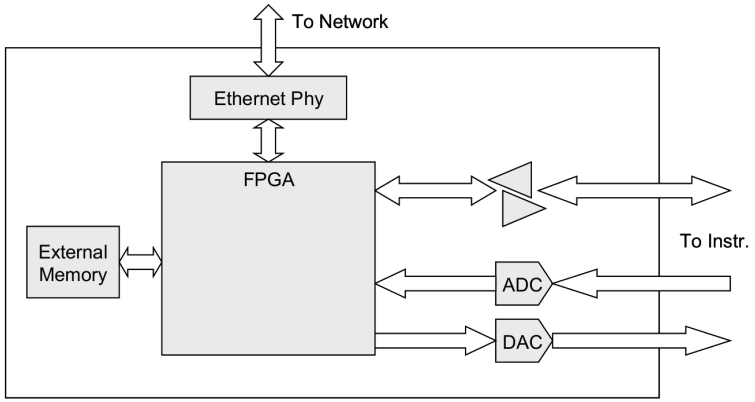


Figure 9: Printed-circuit Board [7]

Types of Embedded Processors

Soft Cores

- HDL Model
- Must Be Synthesized and Fit Into FPGA Fabric

Hard Cores

- Dedicated Physical Component
- Fixed Implementation

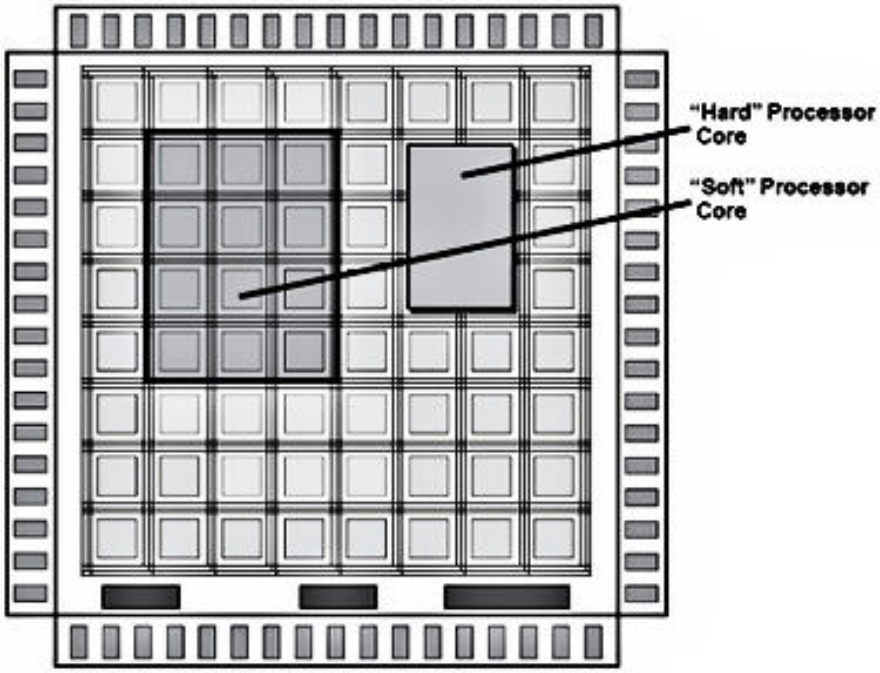


Figure 10: FPGA Embedded Processors (Soft/Hard IP) [13]

[1, 7, 8, 13–18]

Hard vs. Soft Cores

Soft Cores

- *HDL Model*
  - Customizable
  - Synthesis $\rightarrow$ ASIC or FPGA
- must be synthesized and fit into FPGA fabric
  - Flexible (Target Architectures)
  - Obsolescence
  - More Affordable (Source Code)
  - Higher Design Effort
  - Little Documentation
  - Less Optimization
  - Higher Resource Utilization
  - Lower Operating Frequency

Hard Cores

- Dedicated Physical Component
  - Seperate from FPGA's Logic Blocks
  - Higher Operating Frequency
- Fixed Implementation
  - Optimized
  - Low Portability
  - Reliable
  - Good Documentation

[1, 7, 8, 13–18]

Examples of Embedded Processors

Soft Cores

- General Purpose
  - MicroBlaze (Xilinx)
  - Nios II (Altera)
- Open Source
  - AEMB Core (Aeste)
  - OpenRISC1200 (opencores.org)
  - LEON2/3 (Gaisler Research)
- Application-Specific
  - Diamond Standard Series (Tensilica)
  - Xtensa core (Tensilica)

Hard Cores

- PowerPC 405 Embedded Core (IBM) $\rightarrow$ Xilinx Virtex-II Pro and Virtex-4/5 FPGAs
- ARM922T $\rightarrow$ Altera Excalibur FPGAs
- ARM Cortex-A9 Dual-Core MPCore $\rightarrow$ Xilinx Zynq-7000 All Programmable System-on-a-Chip

[1, 7, 8, 13–18]

Off-the-Shelf Processors as Alternative?

Off-the-Shelf Processors

- Lower Device Cost
- Hardware Platform Already Designed
- Mature Software Design Tools

FPGA Embedded Processors

- Component and Cost Reduction
- Less Likely to Become Obsolescent
- Customization
- Hardware Acceleration

[8, 13, 14]

Xilinx Zynq Series

Introduction 03/2011 → First Shipment Q4/2013

[19, 20]

Details on the History of the Devices and Reasons for their Introduction can be found in the Additional Material

FPGA- vs. Processor-centric Approach

FPGA-Centric

- Programmable Logic
- *Optional* On-Chip Processor Extension
- Ex: All Standard FPGAs

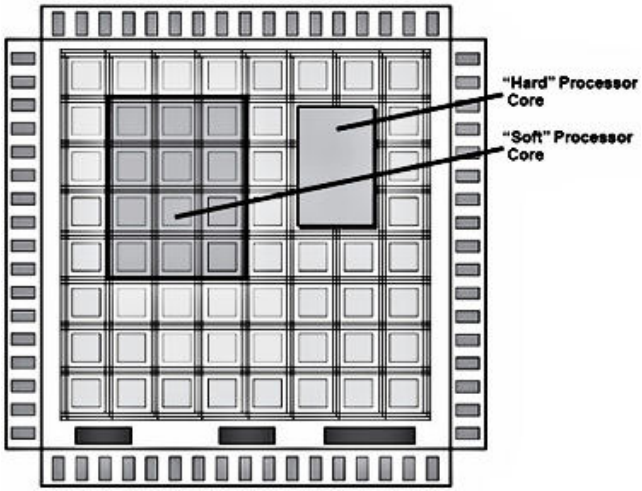


Figure 11: FPGA Embedded Processors (Soft/Hard IP) [13]

Processor-Centric

- FPGA Built Around Processor
- Usually SoC
- Predefined Interfaces

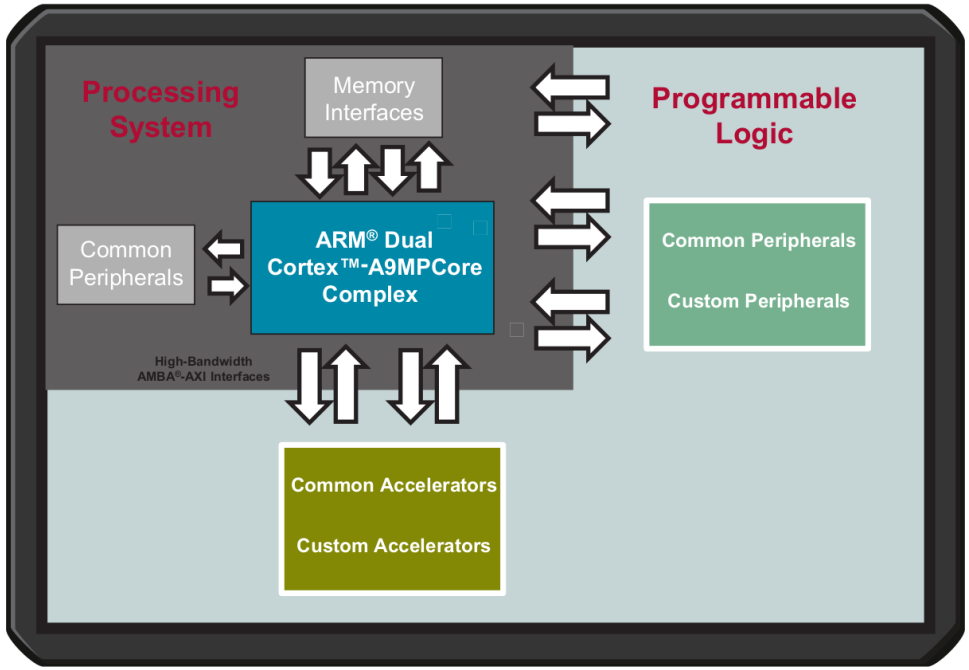


Figure 12: Xilinx' Extensible Processing Platform Architecture [21]

[21–25]

Zynq-7000 – Versions

Zynq-7000 All Programmable SoCs	Automotive-grade XA Zynq-7000	Defense-grade Zynq-7000Q

Figure 13: Xilinx' Zynq-7000 All Programmable SoC Versions [26]

[23, 26–30]

More Details on the Different Versions can be found in the Additional Material

EPP Architecture

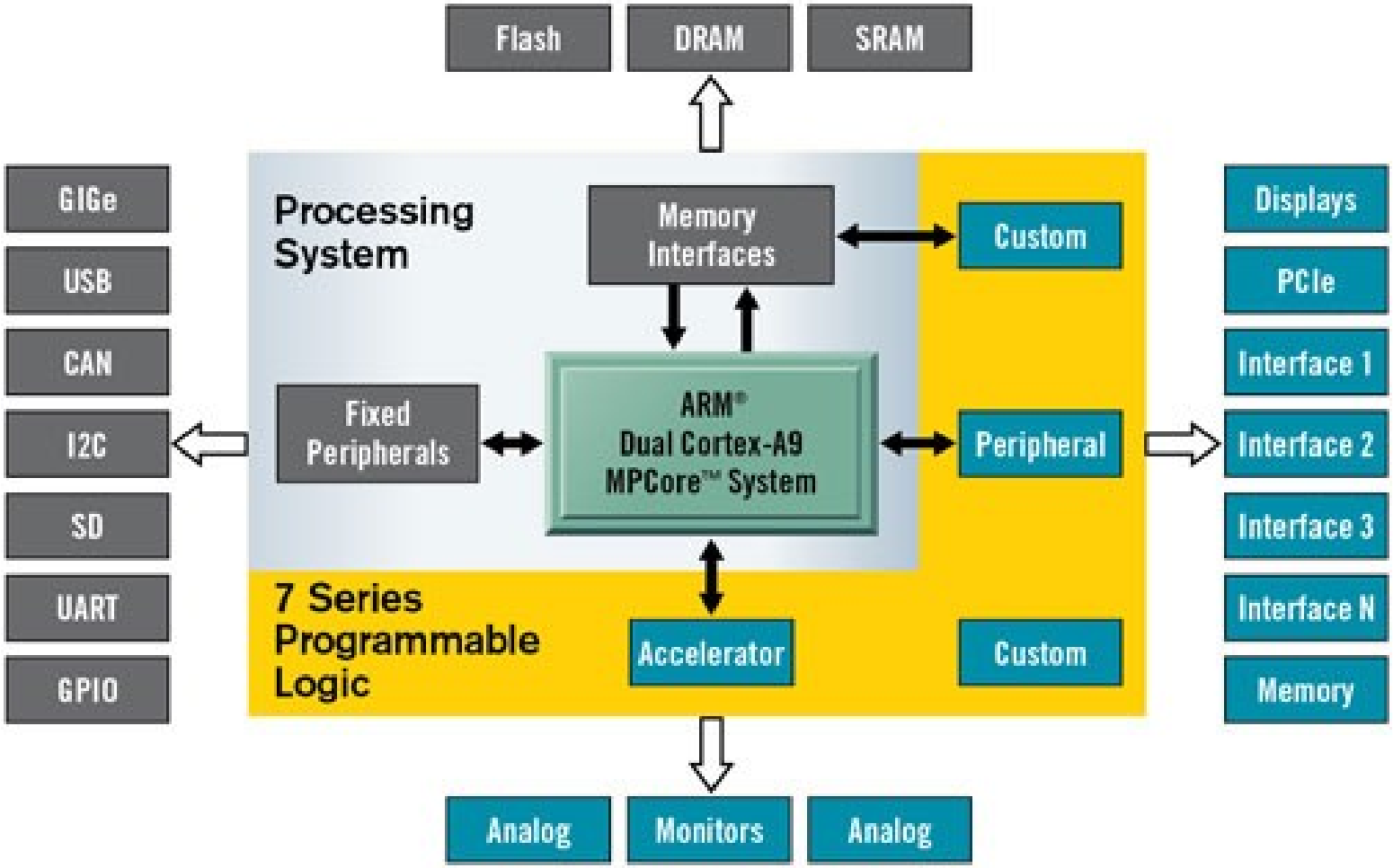


Figure 14: Xilinx' Extensible Processing Platform Architecture [31]

[10, 22–24, 26, 32–34]

Zynq-7000 AP SoC Architecture

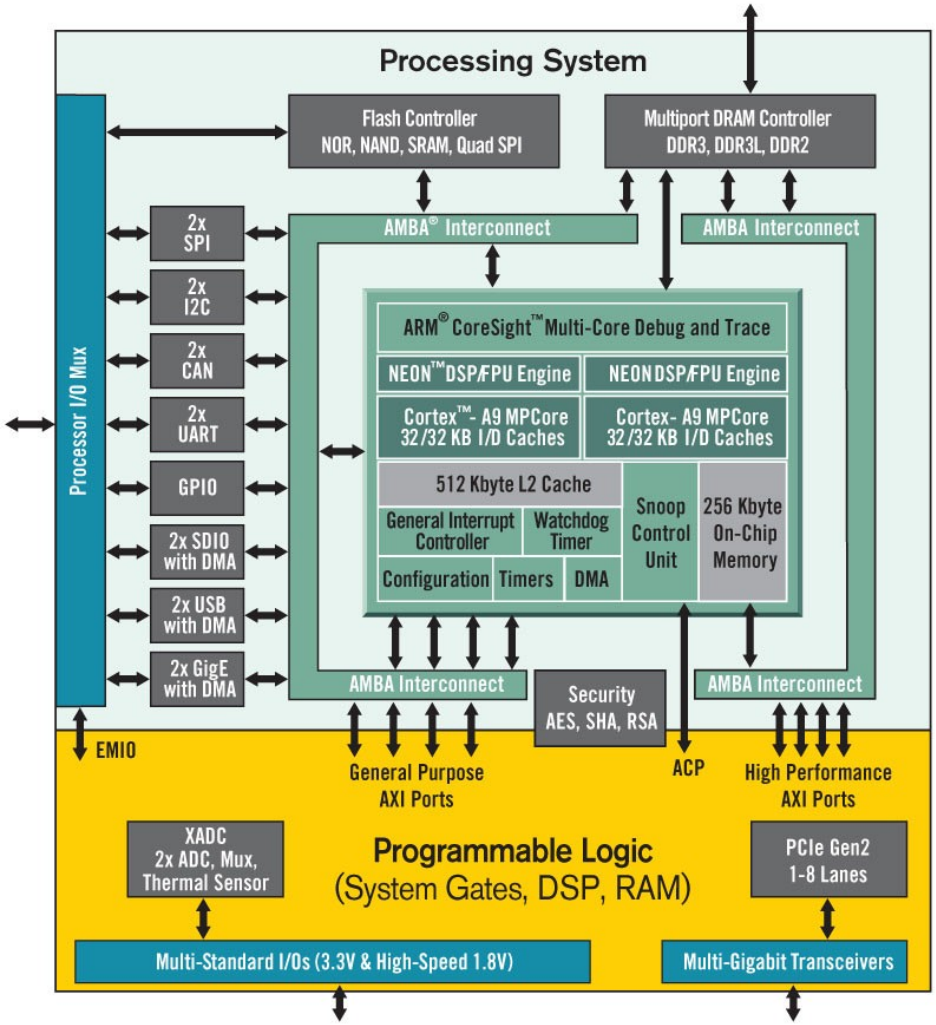


Figure 15: Xilinx' Zynq-7000 All Programmable SoC Architecture [26]

[10, 22–24, 26, 33, 35]

"A Generation Ahead": Performance and Power

High Performance

- ARM Microprocessors
- PS Operating Configurations
  - Both Cores Running
  - One Core Turned Off
- Memory Controllers
- High Throughput Standard Interconnects

Low Power Consumption

- $< 3W/15W$
- Independent Power Supplies $\rightarrow$ Power Modes
  - PL Turned Off
  - PS Clock Control Mode
- Scalable PL (Kintex-7 or Artix-7)

[10, 22, 23, 36]

Performance Evaluation

	Hybrid Devices		**Classical Processor**
	Xilinx	**Altera**	**ARM**
System			
Product	ZC702 Evaluation Platform	Arria V SoCs	ARM11MP 4 Core
Cores	2	2	4
CPU Frequency	$666MHz$	$800MHz$	$732MHz$
Results			
Dhrystone ($DMIPS/MHz$)	2.3	2.5[1]	1.25[1]
Performance ($CoreMarks/Core$)	2369[2]	–	1464
Power Consumption	$< 2W$	$< 1.8W$	–

[10, 23, 37–40]

[1] According to Data Sheet

[2] Z-7020 at $800MHz$

Performance Evaluation

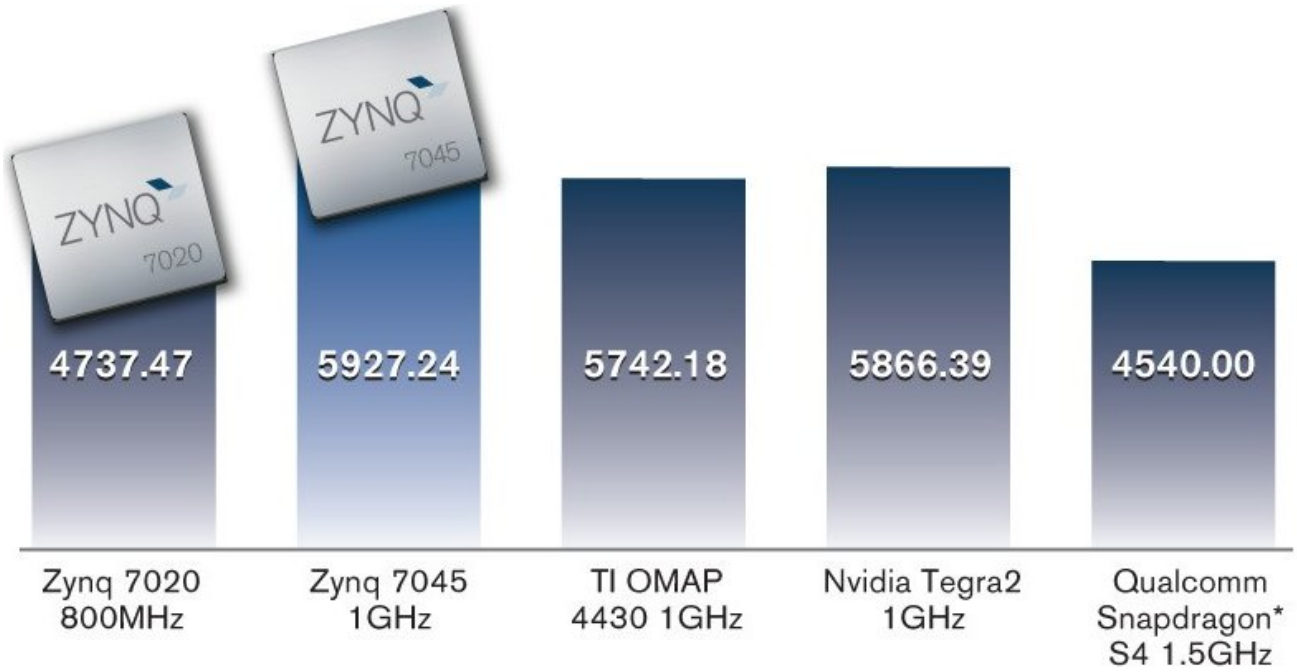


Figure 16: CoreMark Performance Test Done by Xilinx (2013) [41]

DSP Capability	**Z-7100 AP SoC**	**Arria V SoC** (Altera)
Fixed-Point Perf.	$2,622\,GMAC/s$	$1,600\,GMAC/s$ (Arria V FPGA)
Floating-Point Perf.	$778\,GFLOPS$	$300\,GFLOPS$
Transceivers ($10Gb/s$)	16	16
Transceiver Perf.	$10.3123\,Gb/s$	$10.3125\,Gb/s$

[23, 41–45]

"A Generation Ahead": Security and Reliability

- AES and SHA Supported in Hardware
- Boot Sequence
  - Secure or Non-Secure
  - Multi-Stage
- PS: Master $\rightarrow$ Booted Before PL

Figure 17: Zynq-7000 Security Solutions [46]

- Anti-Tamper Technology

[22, 23, 30]

"A Generation Ahead": Productivity

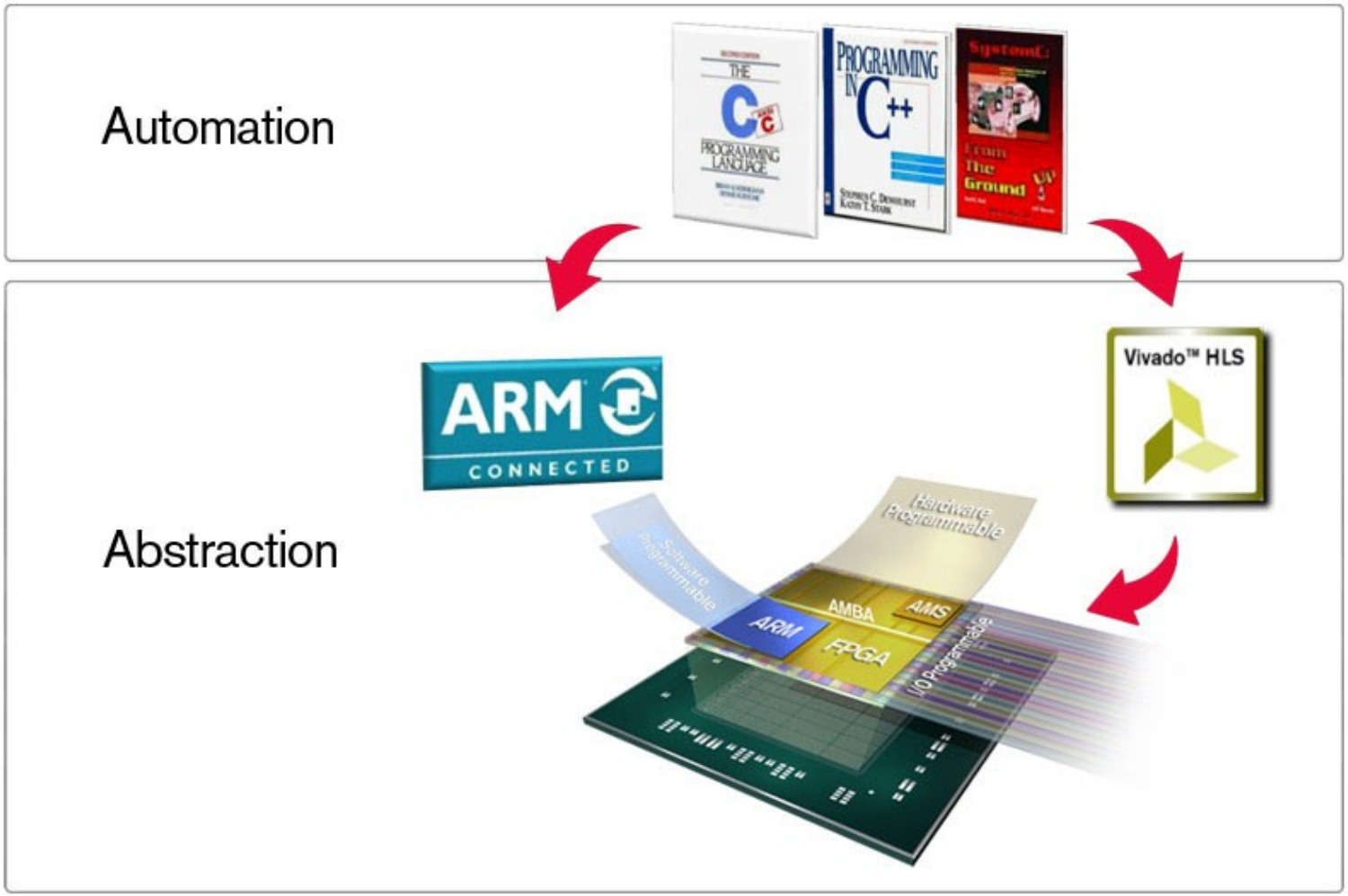


Figure 18: Xilinx' Idea of High-Level-Synthesis [47]

[22, 23, 36, 47]

Application Areas

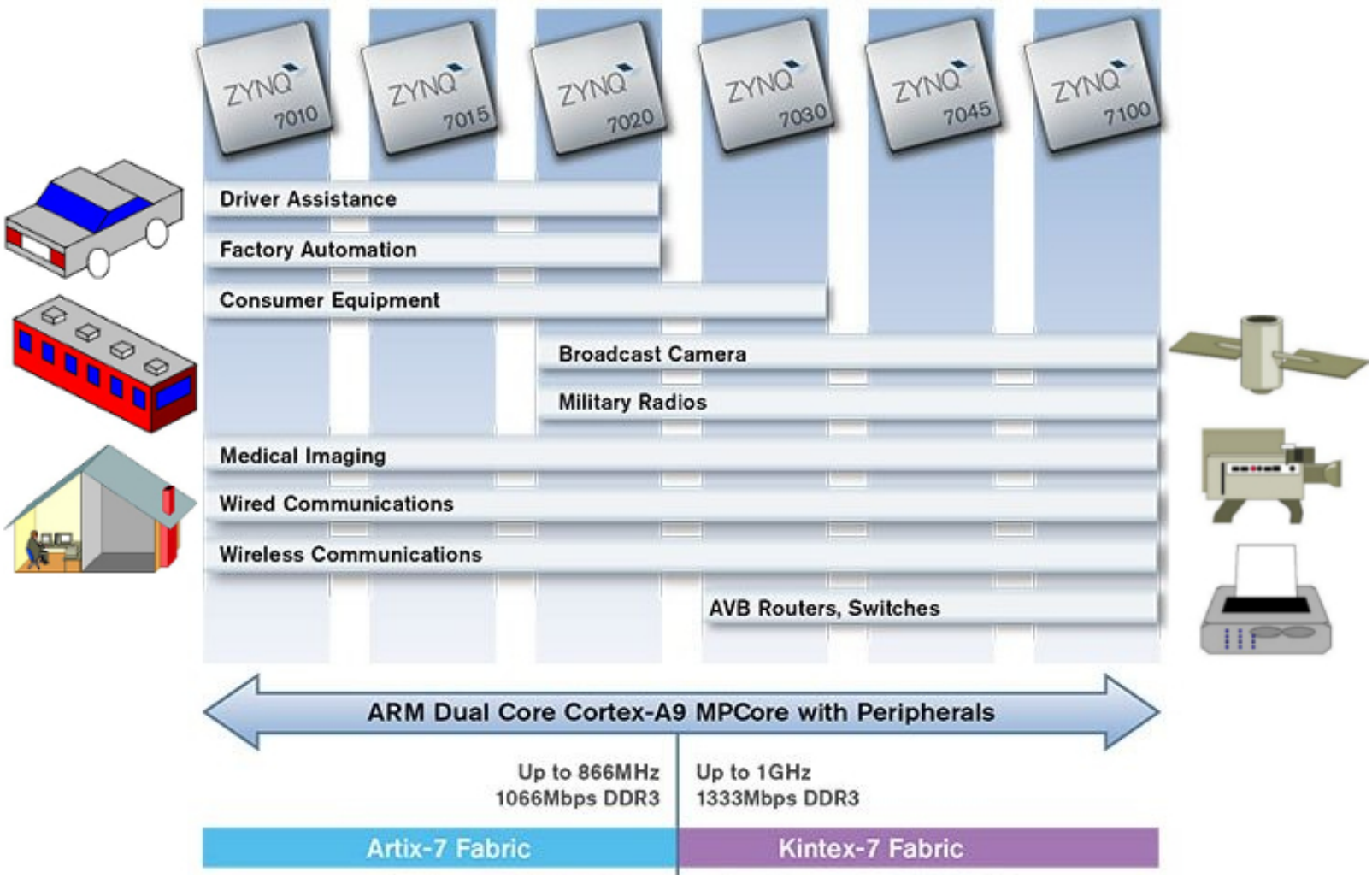


Figure 19: Application Areas of Xilinx' Zynq Series [26]

[21, 22, 26, 30, 31, 41, 48, 49]

Diesel Engine Management

Figure 20: Audi R18 e-tron quattro / ultra (2012) [50]

[50–53]

Customer Opinions

[10, 22, 54, 55]

Competing Products

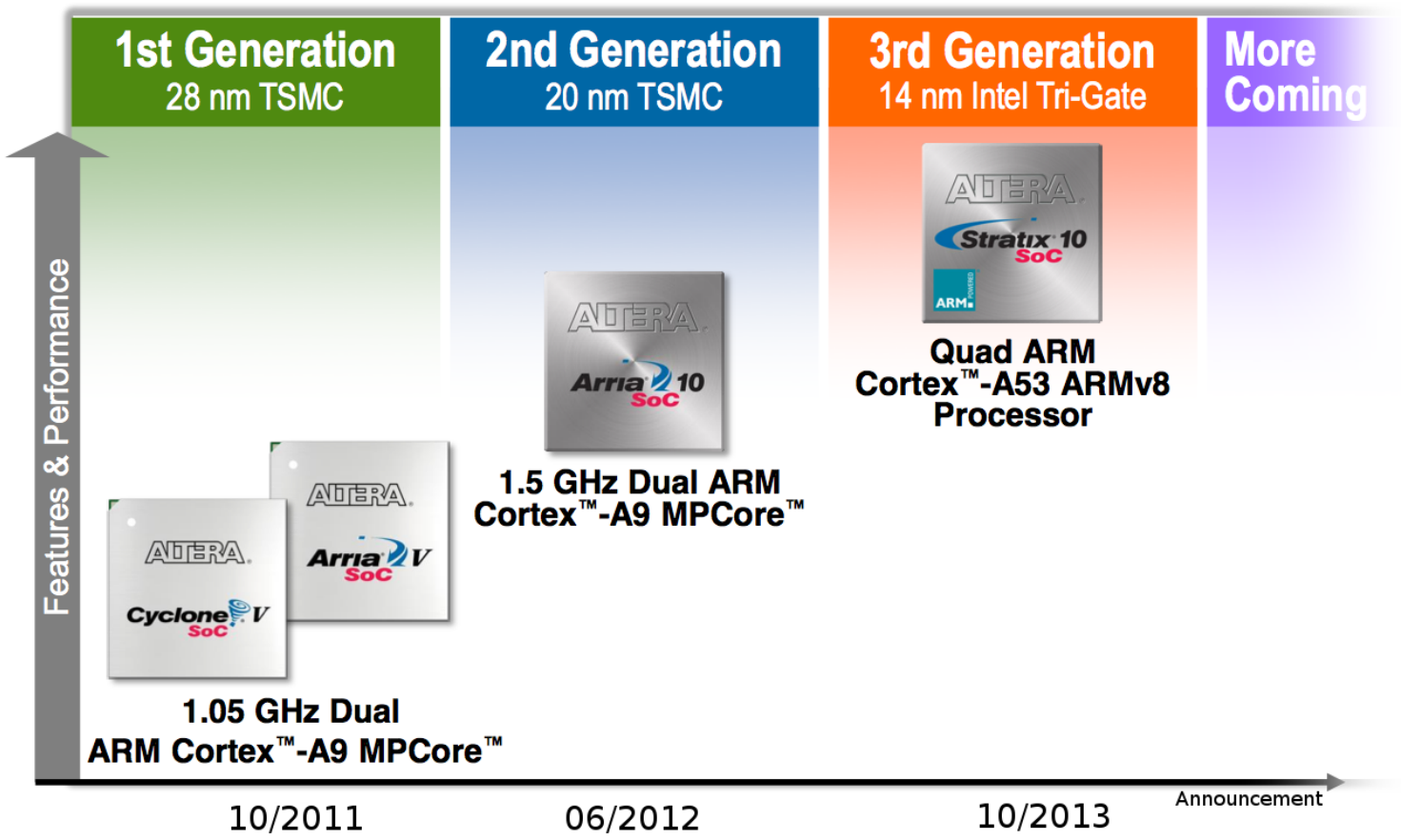


Figure 21: **Altera**'s FPGA SoC Generations [56]

Others:

[25, 44, 49, 57–60]

- **Texas Instruments**: DaVinci SoCs
- **Microsemi**: SmartFusion2 (166*MHz* Cortex-M3)

Xilinx' Reaction

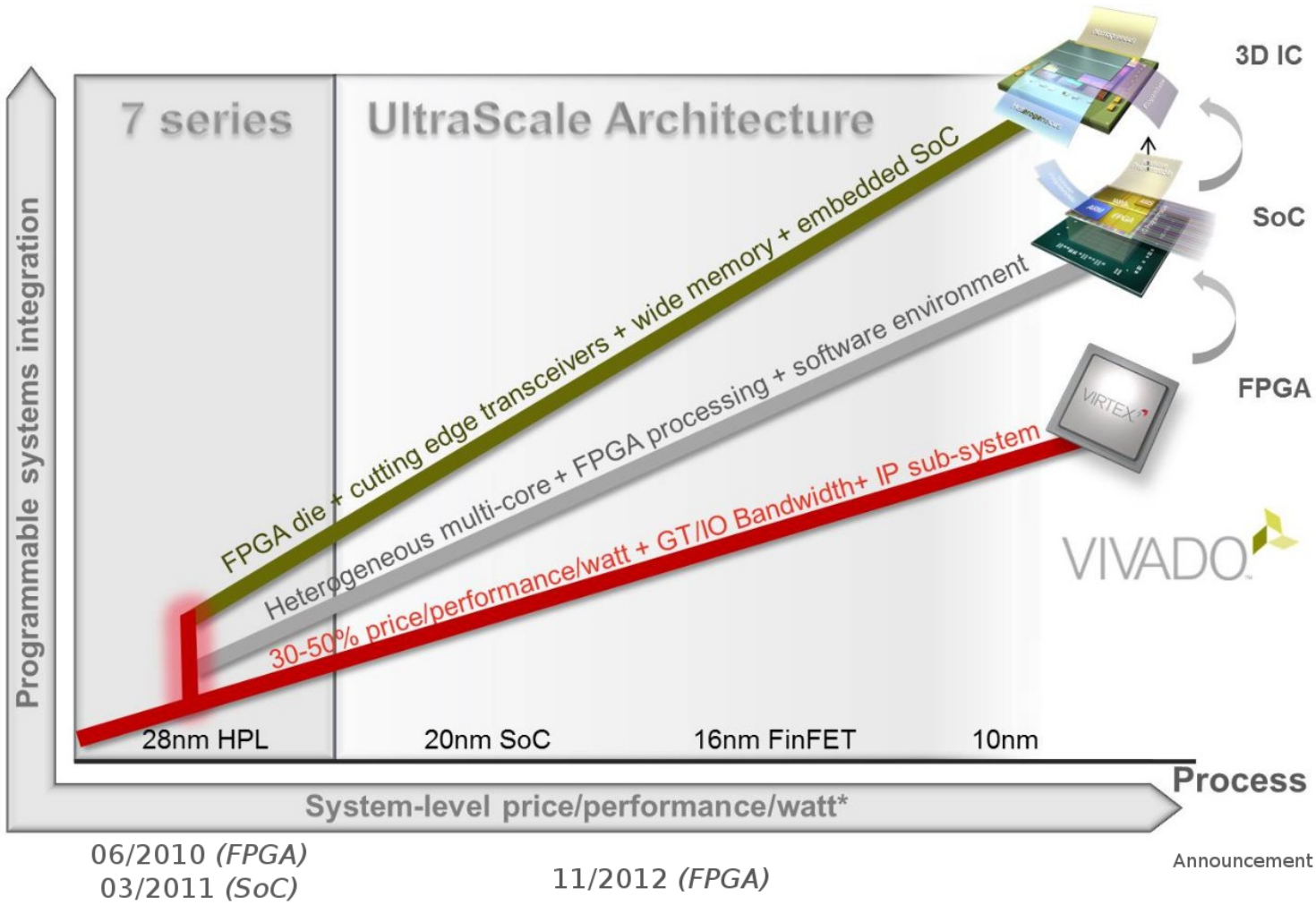


Figure 22: **Xilinx**'s Device Generations [61]

[61–64]

Conclusion – Innovation or Hype?

Progress

- Paradigm Shift: FPGA-centric $\rightarrow$ Processor-centric
- Fast On-Chip L2 Cache
- Snoop Control
- tight coupling: PS – PL (AXI interconnect)
- HLS

Objections

- More Attention on Power Consumption Reduction than Increasing Performance
- AXI Interconnect as System Bottleneck
- Xilinx' Direction Was Good, Altera Going the Same Direction
- Xilinx Resting on Their Laurels?

Conclusion – Innovation or Hype?

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→ **Innovation with Potential!**

Appendix

Xilinx Zynq Series

Figure 23: Examples for Smarter Systems [65]

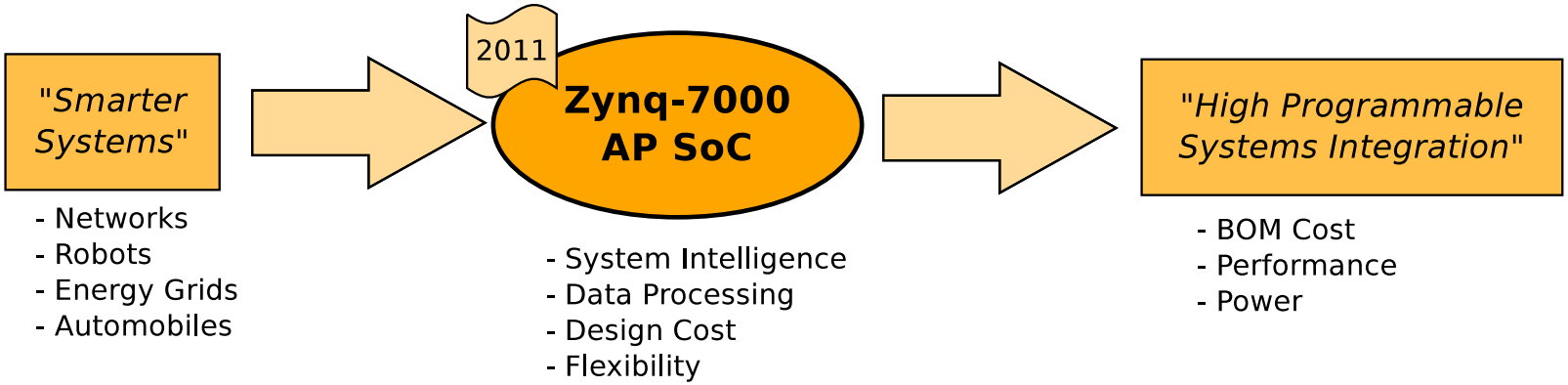

Figure 24: Introduction of Xilinx' Zynq-7000 Series - Reasons and Aims

[22]

Zynq-7000 – Versions

Version	**Zynq-7000 AP SoCs**	**Defense-Grade Zynq-7000Q**	**Automotive-Grade XA Zynq-7000**
Devices	6	2	3
Temp. (min/max)	$-40°C/+100°C$	$-40°C/+125°C$	
Memory Types	All Supported	Some Supported	
Security	RSA, AES, SHA	AES, SHA	
Processor Freq.	$866MHz - 1GHz$	$866MHz$	$733MHz$
FPGA	Artix-7 / Kintex-7	Artix-7	Artix-7 / Kintex-7
DSP	Full Peak Performance	Lower Peak Performance	N/A

[23, 26–30]

Processing System and Programmable Logic

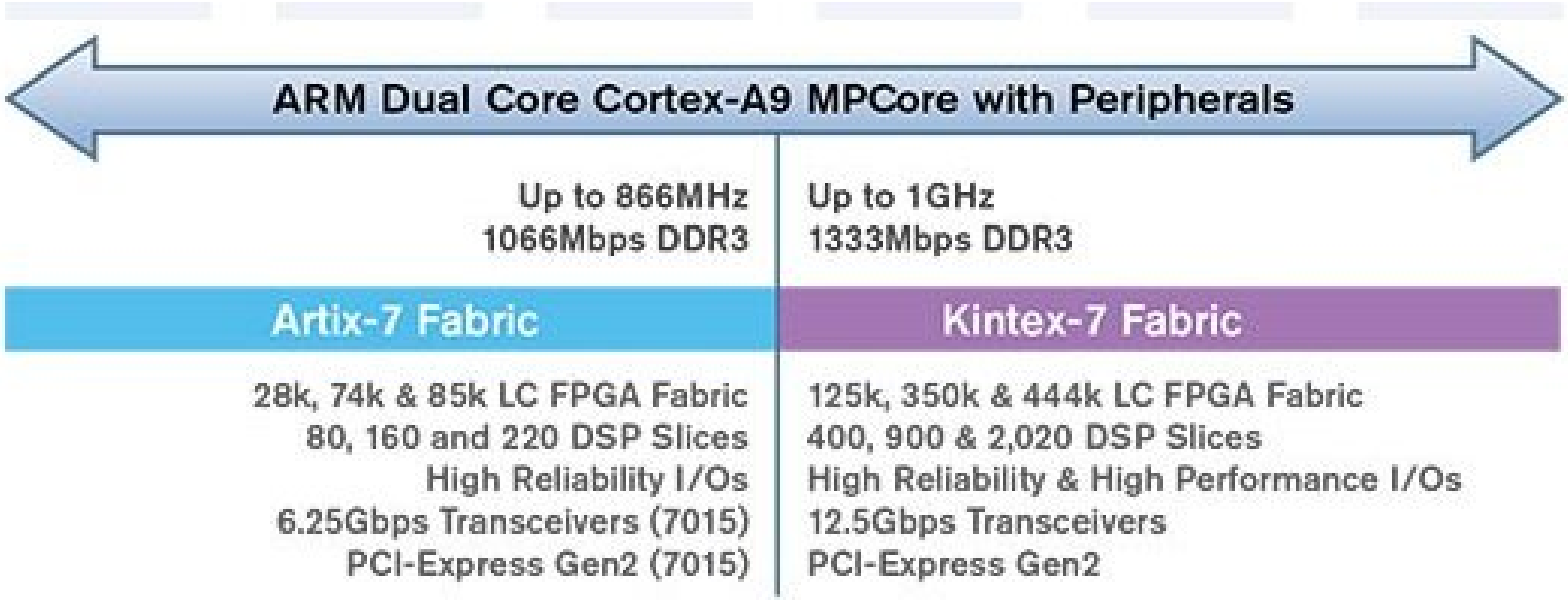

Figure 25: Xilinx' Zynq-7000 AP SoC – Key Figures [26]

[10, 22–24, 26, 33]

"A Generation Ahead": OS, Middleware and Stack Ecosystem

Figure 26: Zynq-7000 SoC Operating Systems [66]

[22, 23, 36]

Reconfiguration

PCAP Instead of ICAP

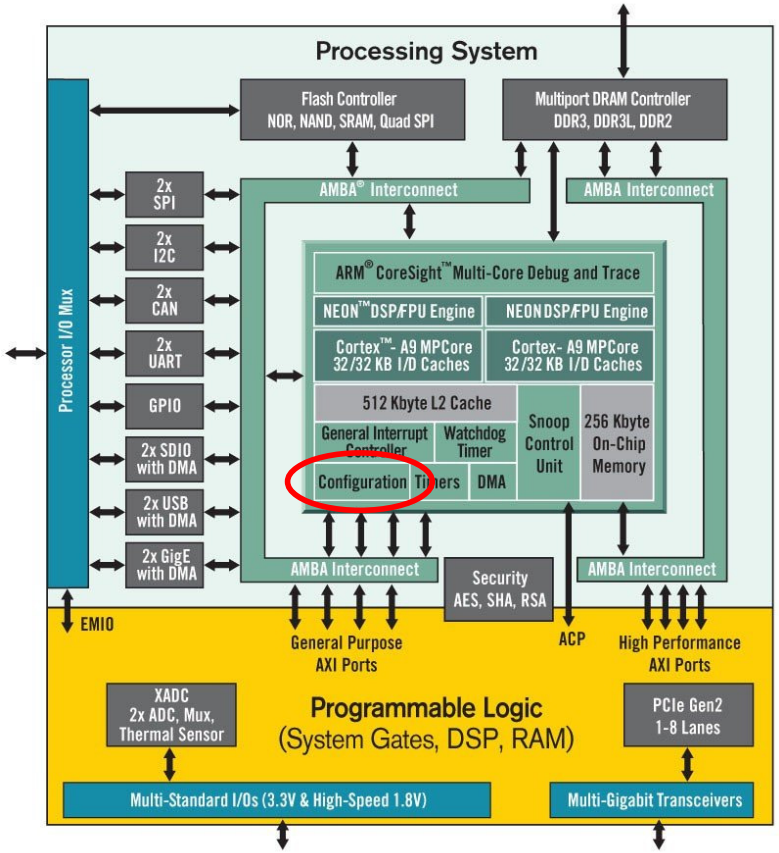

Figure 27: PCAP Location [26]

- Part of PS
- No Instantiation in PL Needed
- PS Can Boot Without PL And Configure It When Needed
- Configuration Bitstream Download via DMA Transfer
- Configuration Frames

[10]

Latest News on Hybrid Devices (2013)

- **Mar**: Zynq-7100 AP SoCs Unveiled [43]
- **Apr**: Xilinx Received Award for Vivado Design Suite [67]
- **Jul**: Developments at Xilinx [49]
  - Full Production of All Five $28nm$ Models in February 2013
  - Sampling of 2^{nd} Generation of $20nm$ Zynq Devices in Fall 2013
- **Sep**: Xilinx Cooperates with NI and MathWorks [68]
- **Oct/Nov**: 1^{st} 64-bit Processor on SoC FPGA [49, 57–59]
  - Alteras Stratix 10 SoCs Contain ARM Cortex-A53 Processor
  - PL Fabricated with Intel's $14nm$ Tri-Gate Process
- **Nov:** Xilinx focuses back on FPGAs without PS [69, 70]
  - Announcement of "Ultrascale Architecture"
  - $20nm - 16nm$ FPGA Fabric
  - Improved Interconnect, Latency and Throughput

Performance Comparison (AXI Interconnect)

Xilinx

Ex: ZC702 Evaluation Kit

- $2x$ 64-bit with $150 MHz \Rightarrow 19.2 Gbps$
- $2x$ 32-bit with $75 MHz \Rightarrow 4.8 Gbps$

[35, 44, 45]

Altera

- more than $125 Gbps$ peak bandwidth ($\rightarrow$ 32-, 64-, or 128-bit data width)

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