Mixed-Signal Design in Chip Development

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Table of Content

What is Mixed Signal Design

- Analog-Mixed-Signal Design(AMS-Design) for integrated circuits (IC) is a combined design work flow for analog and digital circuits in one chip

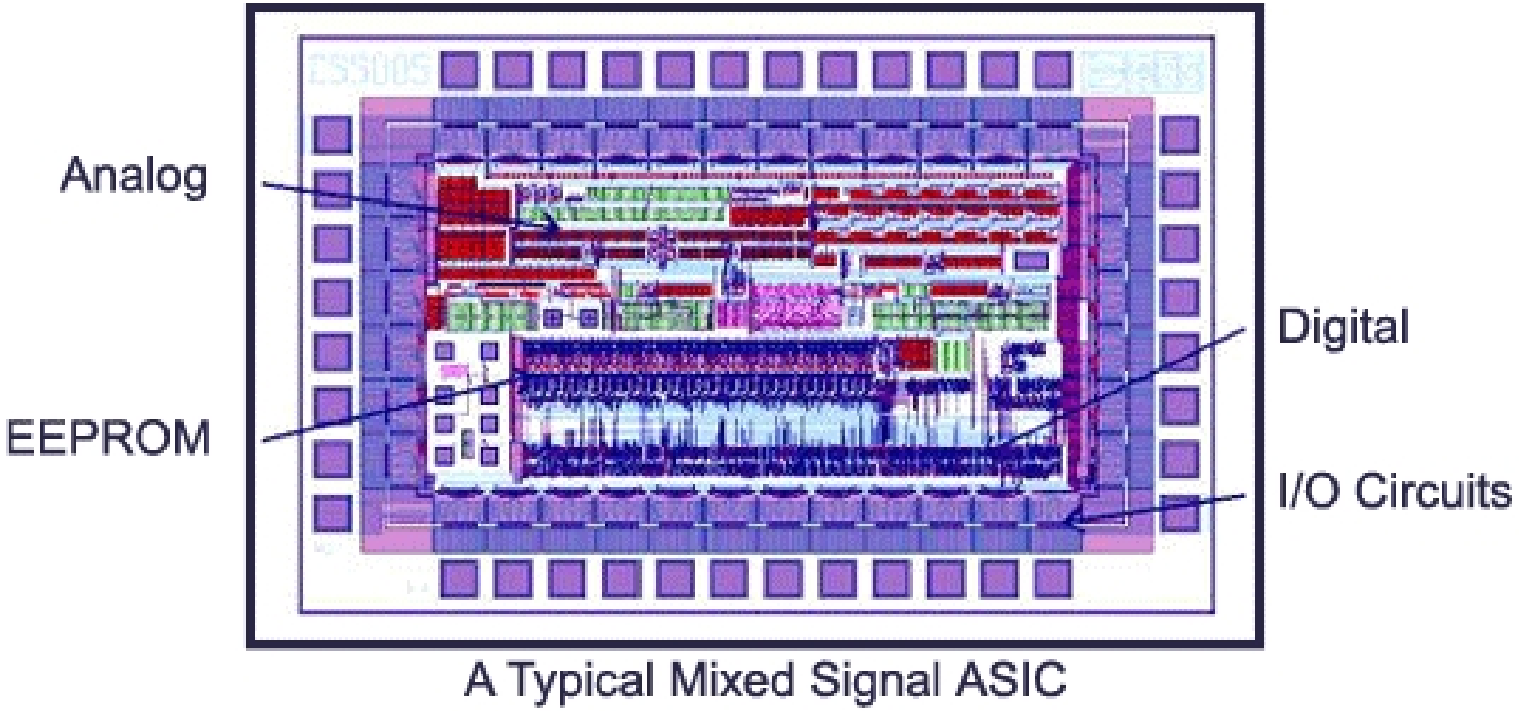


Figure 1 : A typical mixed-signal ASIC[1]

Digital Circuits

- The signal are discrete – low, high, or high impedance
- Consists of integrated MOSFETs to build logic gates and data storage
- Microprocessors, FPGAs, memories
- Simulation event driven, very fast
- Libraries for modules
- Register Transfer Level (RTL) to build complex modules such as FIFOs or adders

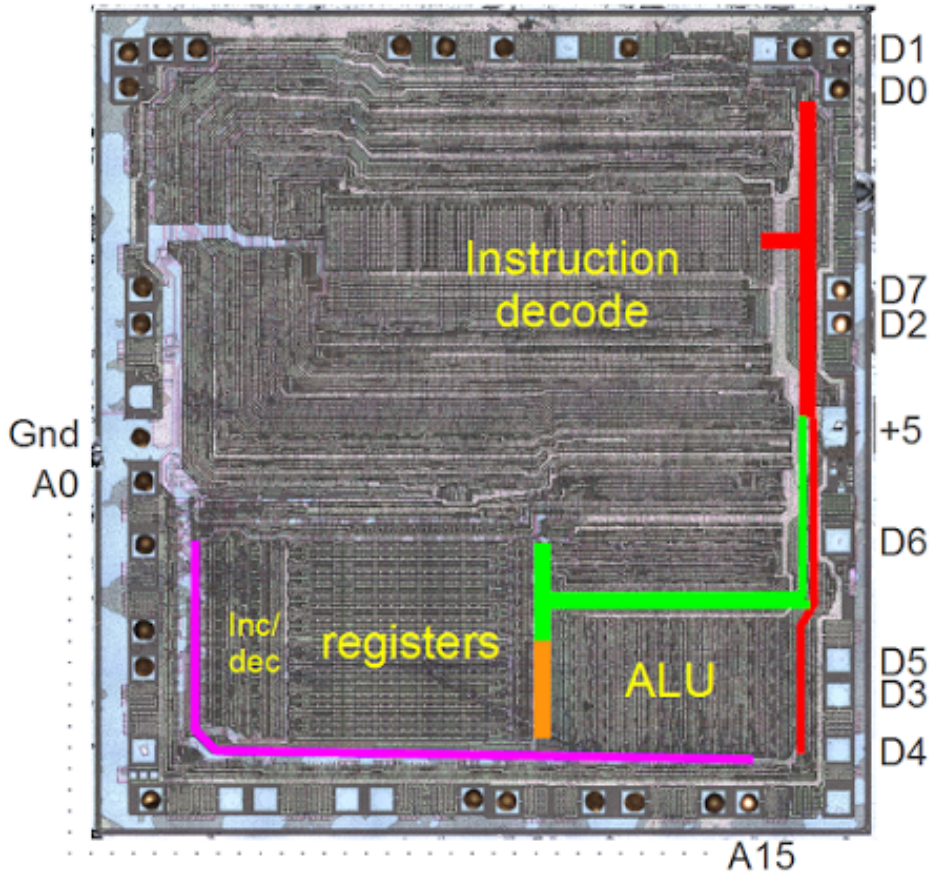


Figure 2 : Photo of the Z80 die. (address bus - purple, data buses red, green, and orange) [2]

Analog Circuits

- The signal contains information using non-quantized variations in frequency and amplitude
- Consist of linear components like capacitors or resistors
- Op-amps, active filters, Phase Lock Loops (PLL)
- Simulation depend on interaction between components, factor 1000 slower than digital simulation

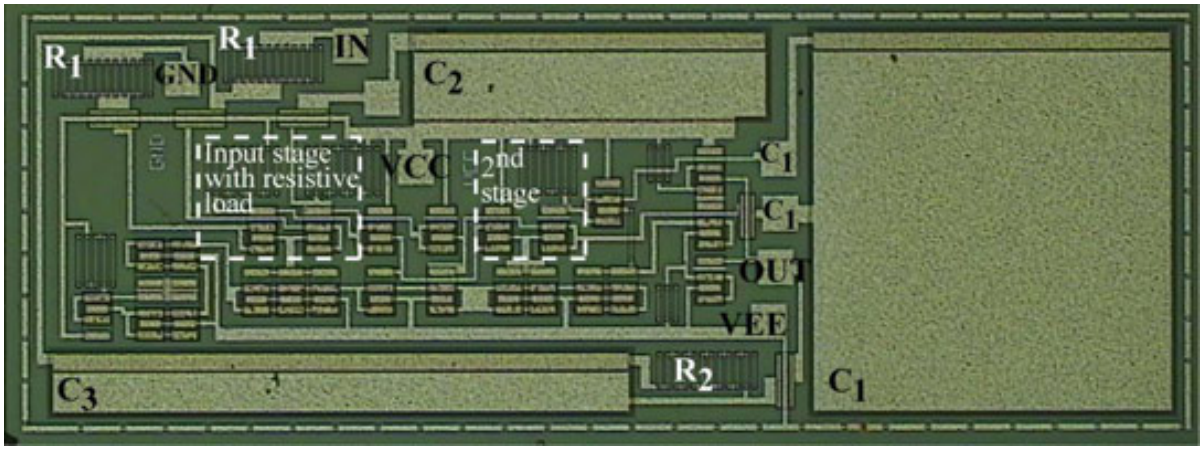


Figure 3 : opamp with integrated feedback resistor (total area ~3.75mm2)[3]

[4]

Problems with Analog Libraries and Analog IP

- A digital library grow with time, reuse of verified modules in later projects
- Analog libraries:
  - small circuits consist quickly of many components
  - each component has its own value and influence the whole behavior
  - make all variable is not possible because the behavior can change dramatical
  - many circuits variations for one function (voltage, current, capacity, resistance, etc.)
- Analog IP:
  - the vendor say all works and is verified
  - does the vendor provide the verification documentation and test benches $\Rightarrow$ verify analog IP contend on your own need much time

Why is Mixed Signal Design Important Today

- Current development aims to integrate all components in one Chip – System-on-a-chip (SoC)
  - leads to analog and digital functions in one chip
  - interferences between analog and digital circuits (chip planing)
  - increase verification work, how to simulate ? analog ? digital?

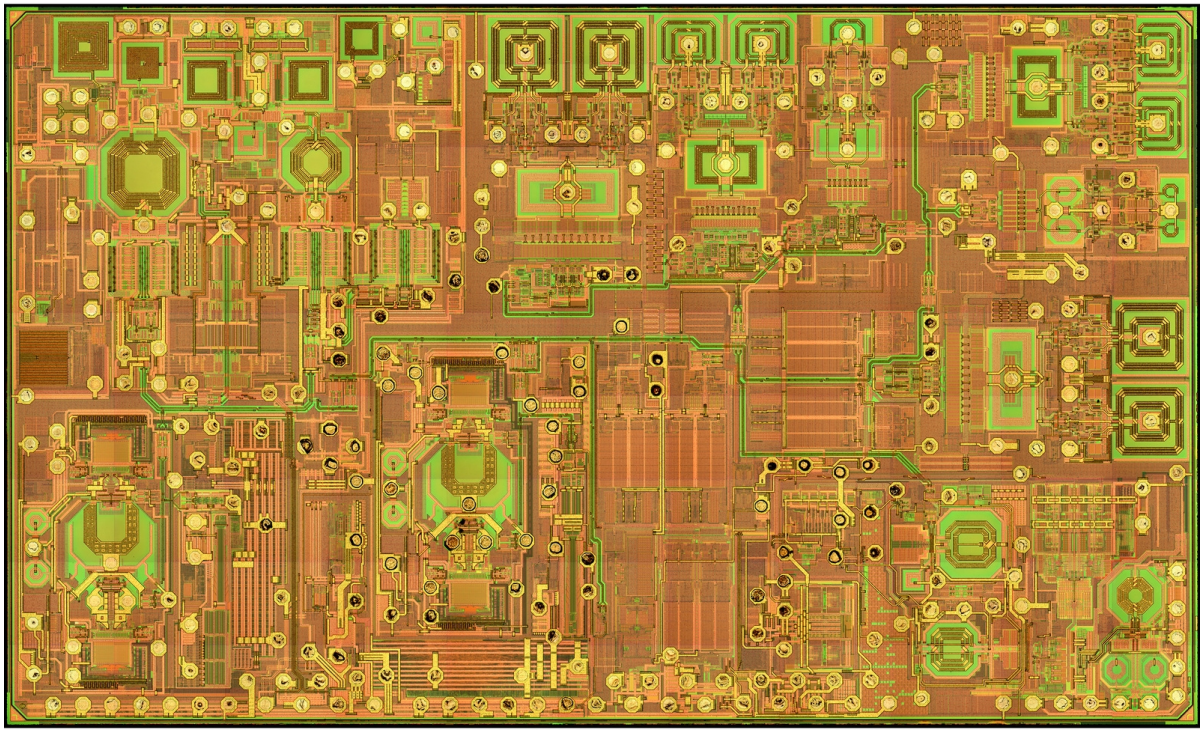


Figure 4 : Qualcomm RTR8600 multi-band/mode RF transceiver[5]

Work Flow before the Mixed Signal Approach

- Interfaces between digital and analog teams and own work flow
- Interferences in communication and specification leads in faults and re-spin

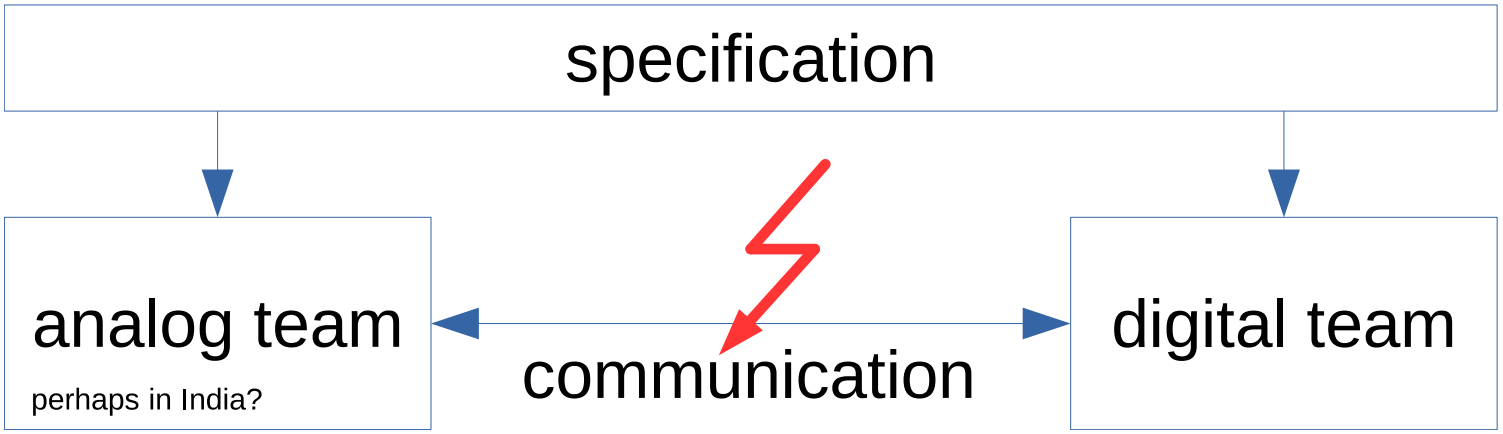


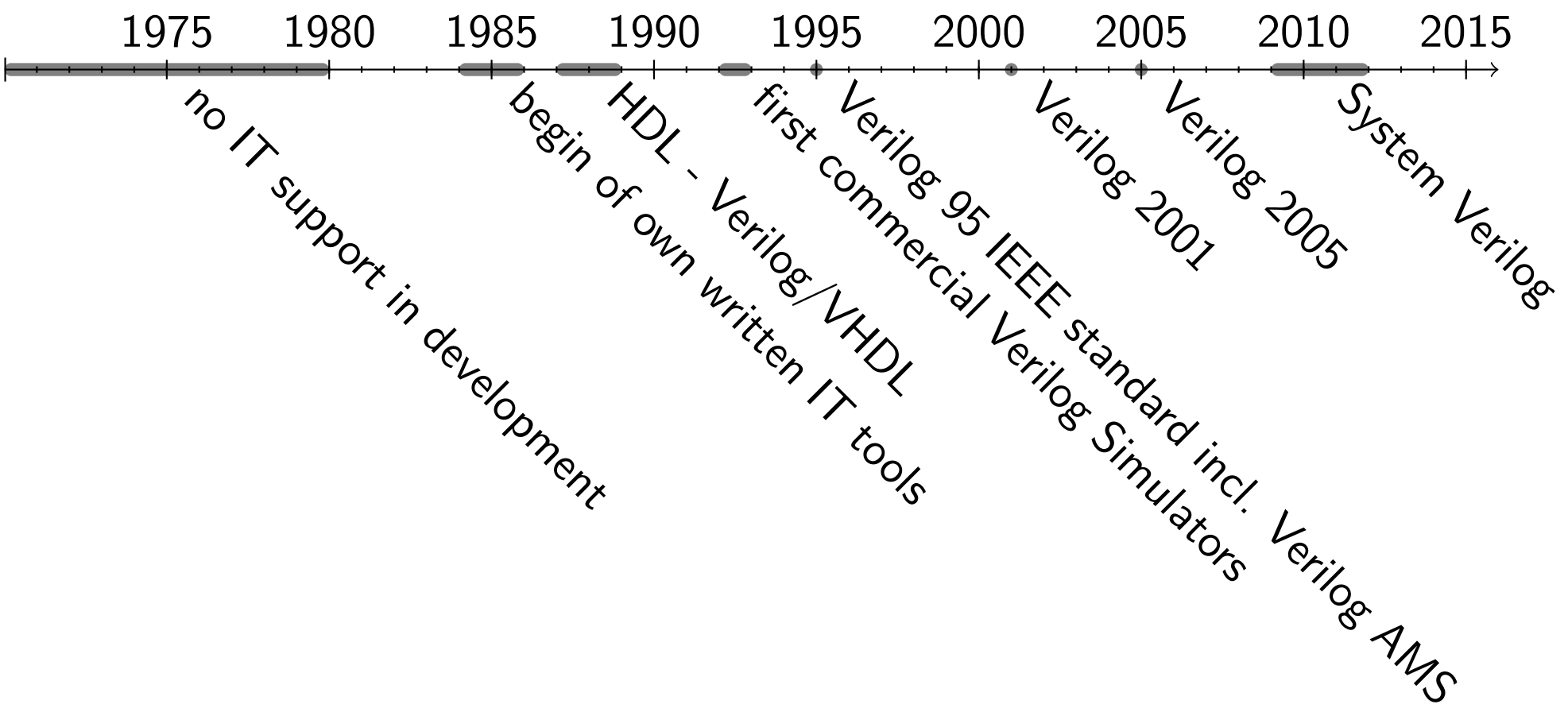
Figure 5 : example for work split

Advantages of Mixed Signal Design

- The mixed signal approach combine analog and digital design
  - reduce the verification time
  - faster time to market
  - avoid re-spin
    $\Rightarrow$ save money, time and missed market opportunities
- Challenges
  - analog simulation is the bottleneck in verification because time intensive calculations for high accuracy
    $\Rightarrow$ using of models
  - low power techniques: several modes (suspend, sleep, eg) $\Rightarrow$ more verification cases

[6–8]

Computation Support in Chip-Development - Time Line



[9, 10]

Design Methodologies

- Top-down and Bottom-up
- Analog-Centric Mixed Signal Flow
- Digital-Centric Mixed Signal Flow
- Unified, Concurrent Approach

Top-down - Digital

- Specification
  –> interfaces
  –> requirements for functional components
  –> implementation
- System level verification, concurrent implementation

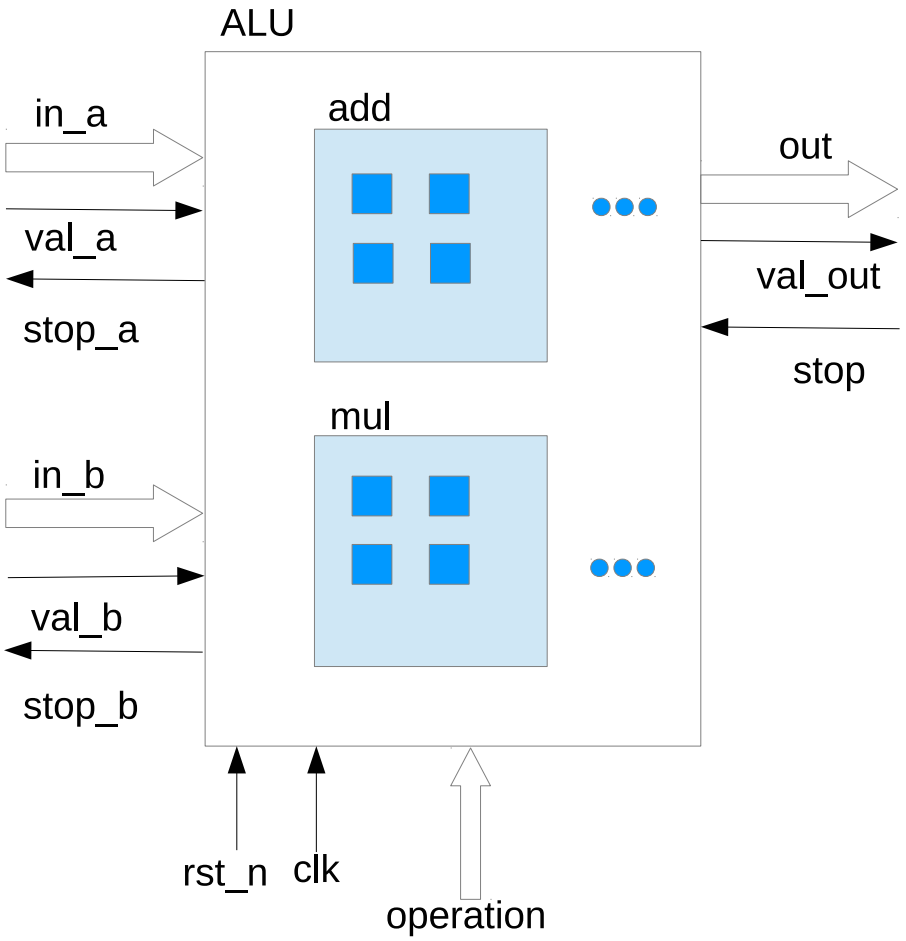


Figure 6 : top-down design for a alu

Bottom-up - Analog

- Design individual blocks on transistor level –> verification of blocks
- Most circuits already exist –> tuning to meet specification
- Combine blocks to form the system –> custom design to achieve performence contraints
- Challenge: system level reached late in design cycle –> architectural changes to increase performance difficult

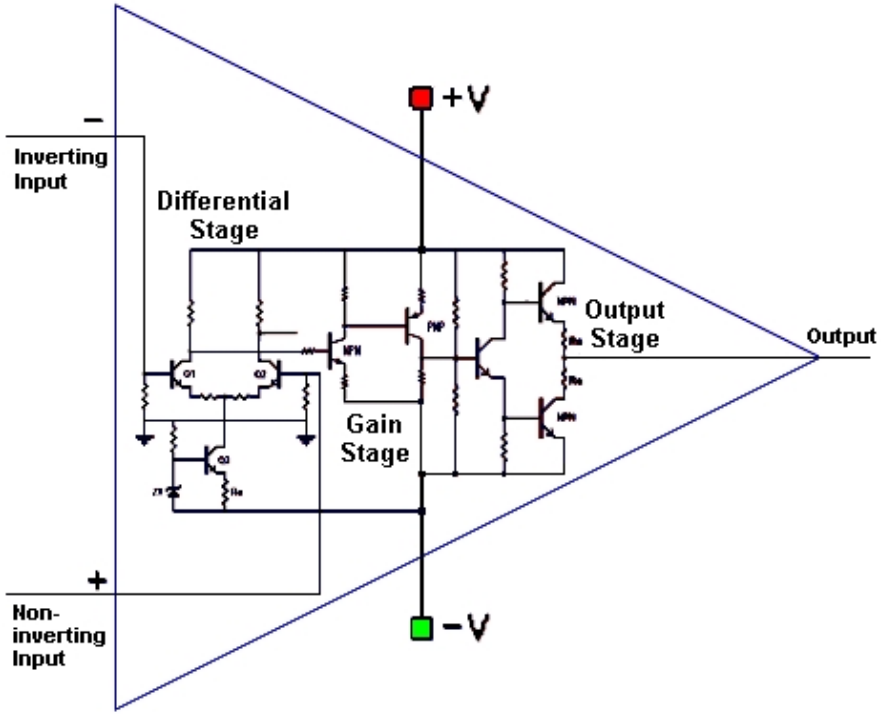


Figure 7 : opamp circuit[11]

Analog-Centric Mixed Signal Flow

- Main parts are analog and a few digital functions are included
- Schematic editor is then main used tool
  - creating layout
  - build test benches
  - run simulations
  - optimizations

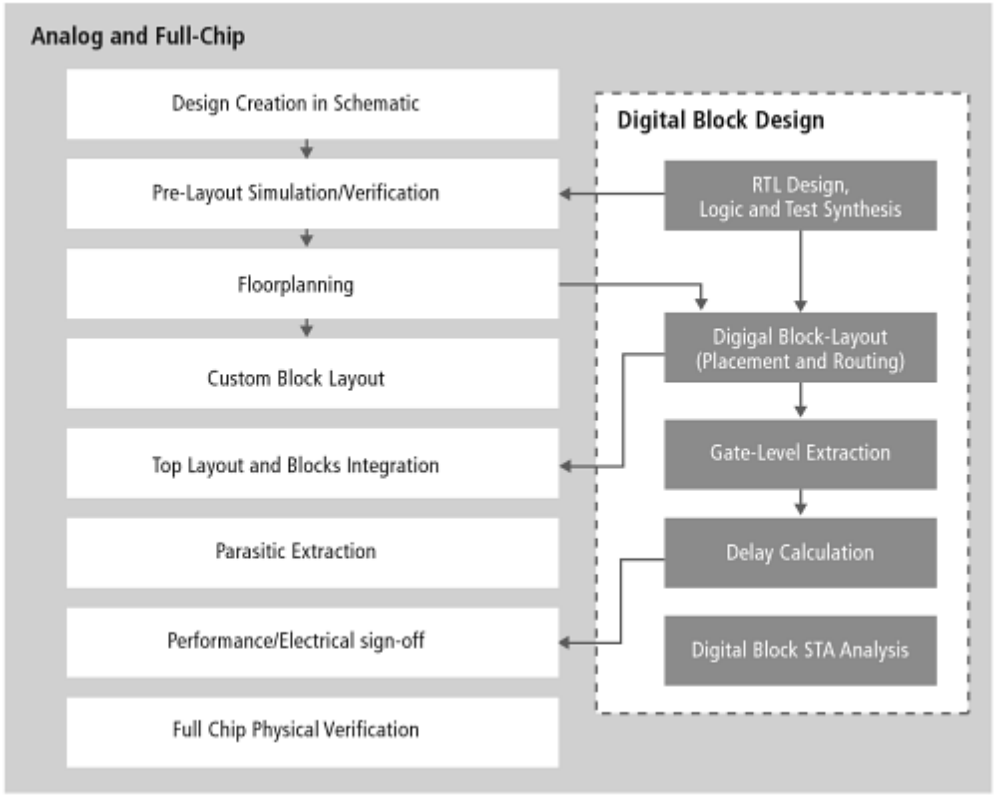


Figure 8 : analog centric workflow [8]

Digital-Centric Mixed Signal Flow

- Main parts are digital and a few analog modules
- Analyzing the analog module timing to integrate in digital verification
- Starts at high level of abstraction
- Static Timing Analysis (STA)
  - computing timing without simulation
  - checks the design only for proper timing
  - not for correct logical functionality

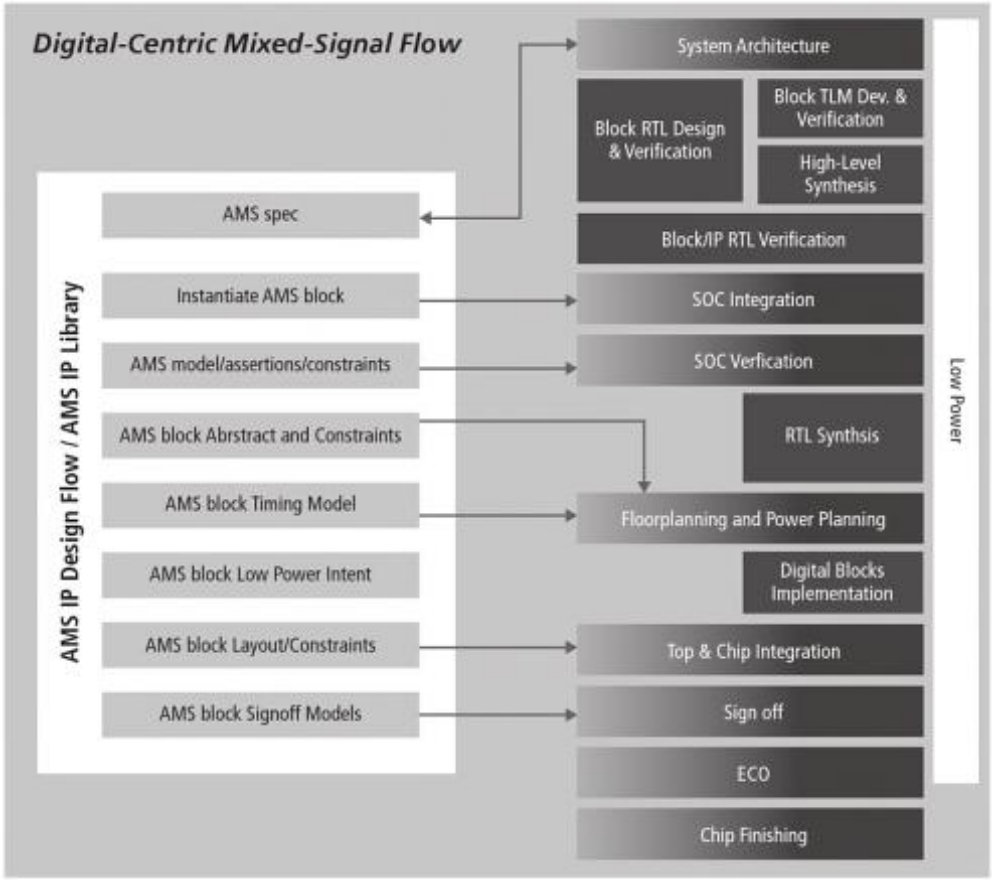


Figure 9 : digital centric workflow [8]

Unified, Concurrent Approach

- Co-design and verification
- Abstraction of the analog functions is inevitable
- Central role: database realized in Open Access
- Design intent is clearly defined by constraints throughout all design stages
- White instead of black boxes

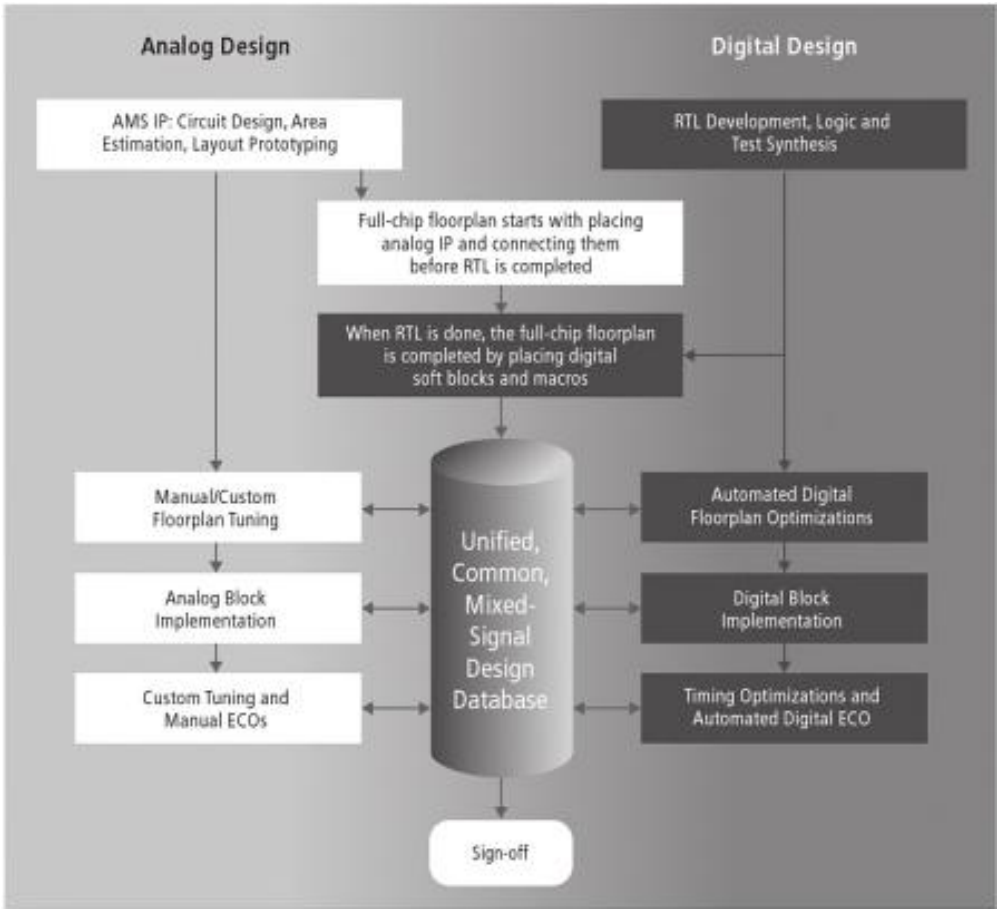


Figure 10 : concurrent workflow [8]

How to Choose the Methodology for a Project

- Identify the main focus of the project, size of design, analog-digital interfaces
  - analog parts dominate with some digital standard cells
    $\Rightarrow$ analog centric
  - digital parts dominate with some analog IP or pre existing modules
    $\Rightarrow$ digital centric
  - heavy mixed designs with many digital and analog blocks being co-designed in parallel
    $\Rightarrow$ concurrent mixed design
- Critical components determine some specifications (bottom up analysis - serializer for example)

Brief Overview of Development Environments

- EDA - Electronic Design Automation
- Best known commercial development environments
  - Synopsys
  - Cadence
  - Mentor Graphics, Zuken Inc., Dolphin Integration, Tanner EDA, Keysight (EEsof), Silvaco
- Open source
  - Alliances
  - gEDA
  - manual toolchain

Synopsys - Custom and Mixed Signal Design Solution (1/2)

- integrated suite of tools for mixed-signal SoC design
- Addressing all aspects of SoC design
- Native support for OpenAccess
- Compliant with industry standard interoperable PDKs
- Access to large mixed-signal IP portfolio
- Integrated physical (signoff) verification and parasitic extraction

[12]

Figure 11 : Synopsys tool chain [12]

Synopsys - Custom and Mixed Signal Design Solution (2/2)

- Highest performance mixed-signal simulation
- Advanced AMS regression and analysis environment
- Industry-reference, high performance SPICE and FastSPICE simulators

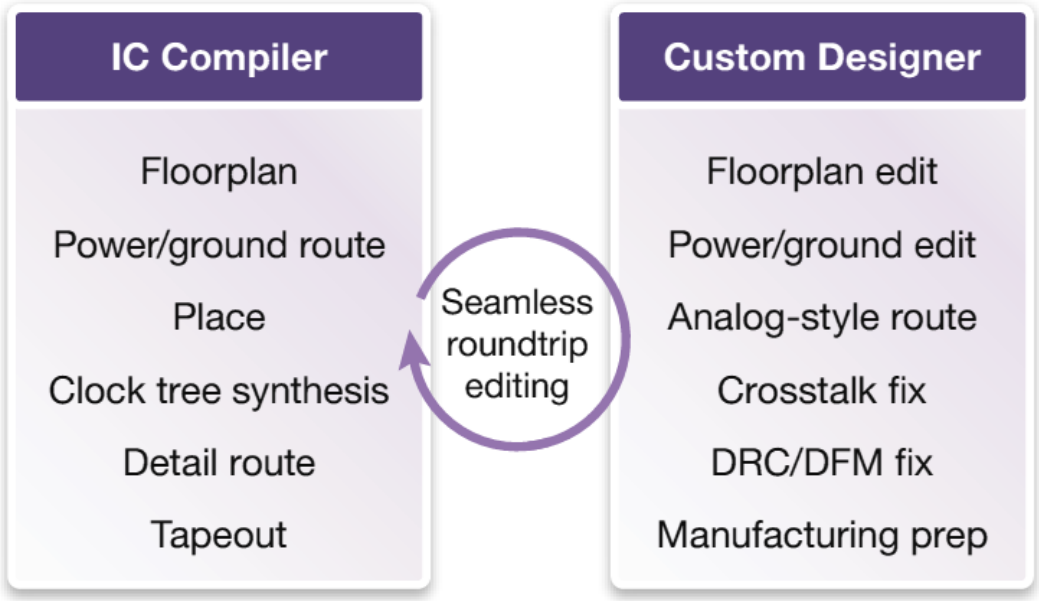


Figure 12 : IC Compiler Custom Co-Design[12]

Cadence - Virtuoso / EDI

- Concurrent, OpenAccess-based Mixed Signal Implementation
- Mature, proven analog and digital design platforms
- Orientated for splited teams (analog/digital)

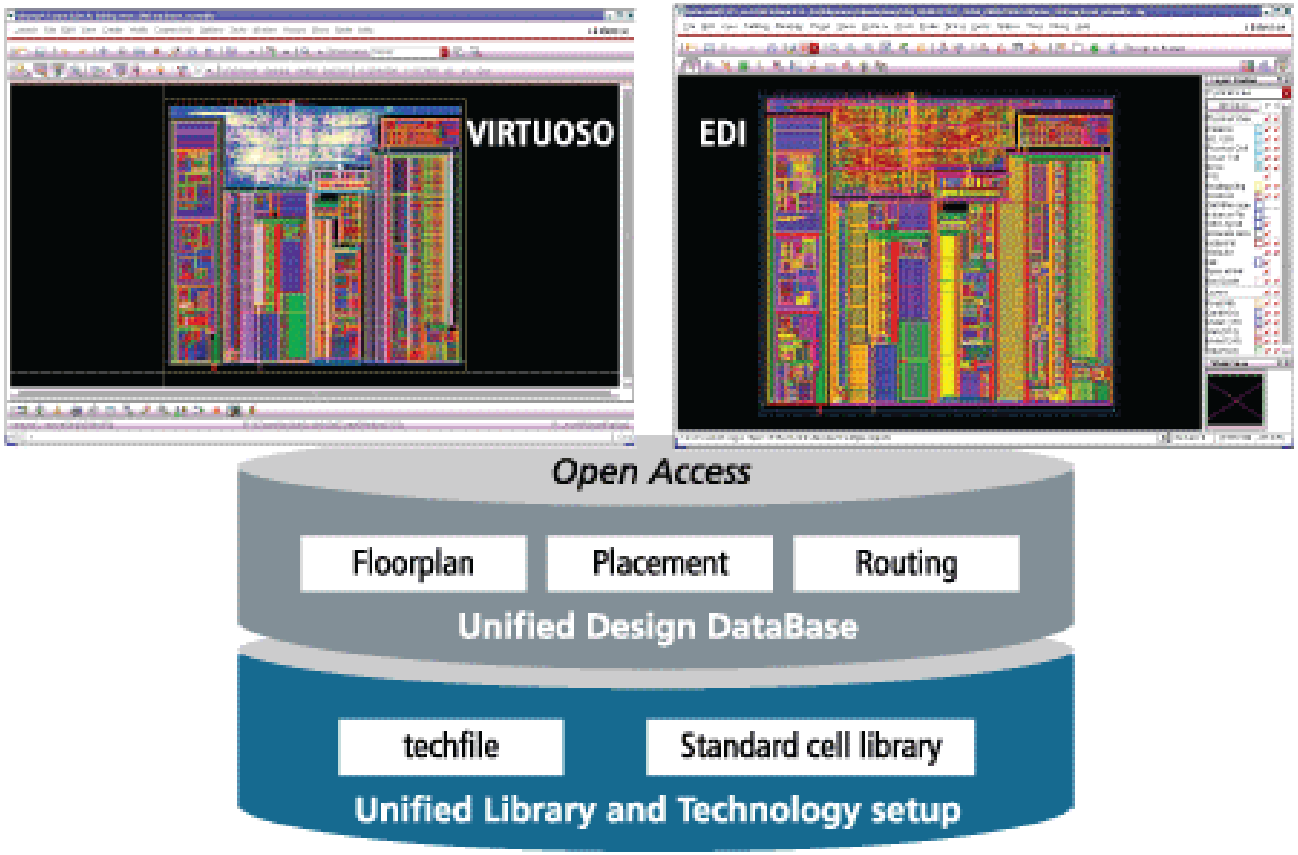


Figure 13 : Cadence Virtuoso / EDI[13]

Other Vendors

- Mentor Graphics, Zuken Inc., Dolphin Integration, Tanner EDA, Keysight (EEsof), Silvaco
- Own editors and simulators
- Most have support for mixed design and verification like Synopsis and Cadence
- All have PDK and IP support
- Many acquire in last time

Open Source

- Alliances, Department for SoC at Pierre et Marie Curie University - Paris
  - tools for multiprocessors system on chip design
  - architectures, methods and tools for the modelling, the simulation, the design and the verification of mixed and heterogeneous circuits
- gEDA
  - gEDA/gaf – schematic capture and netlisting
  - ngspice/gnucap – SPICE/analog simulation
  - gspiceui – GUI front end for ngspice/gnucap
  - pcb/gerbv – PCB layout/ Gerber viewer
  - Icarus Verilog – Verilog simulator
  - GTKWave – Digital waveform viewer
  - wcalc – Transmission line and electromagnetic structure analysis
- Open Circuit Design: Magic, Netgen, Qrouter, Qflow

[14–16]

Practical Demonstration - AMS Behavior Modeling

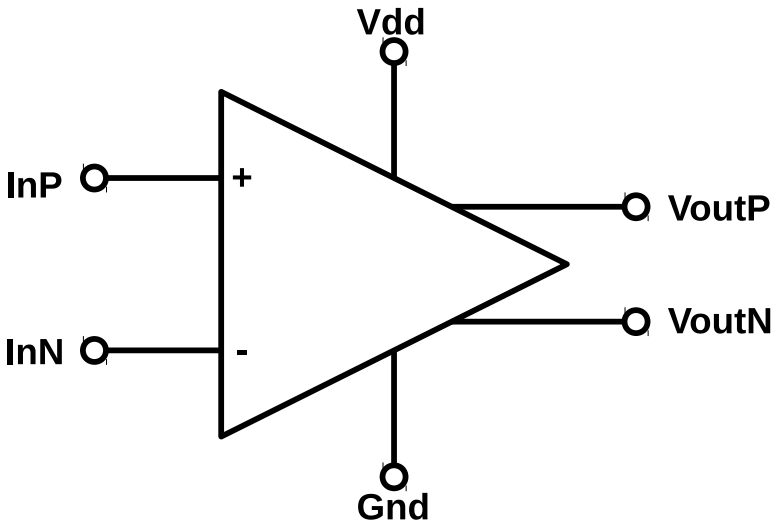


Figure 14 : differential output-stage

Differential Output Stage

- Analog designed differential-output- stage
- Convert digital signals (1/0/Z) in analog signals (voltage level)
- Key facts: voltage, current, slew rates, frequency, Power supply rejection ratio (PSRR), Common mode rejection ratio (CMRR)

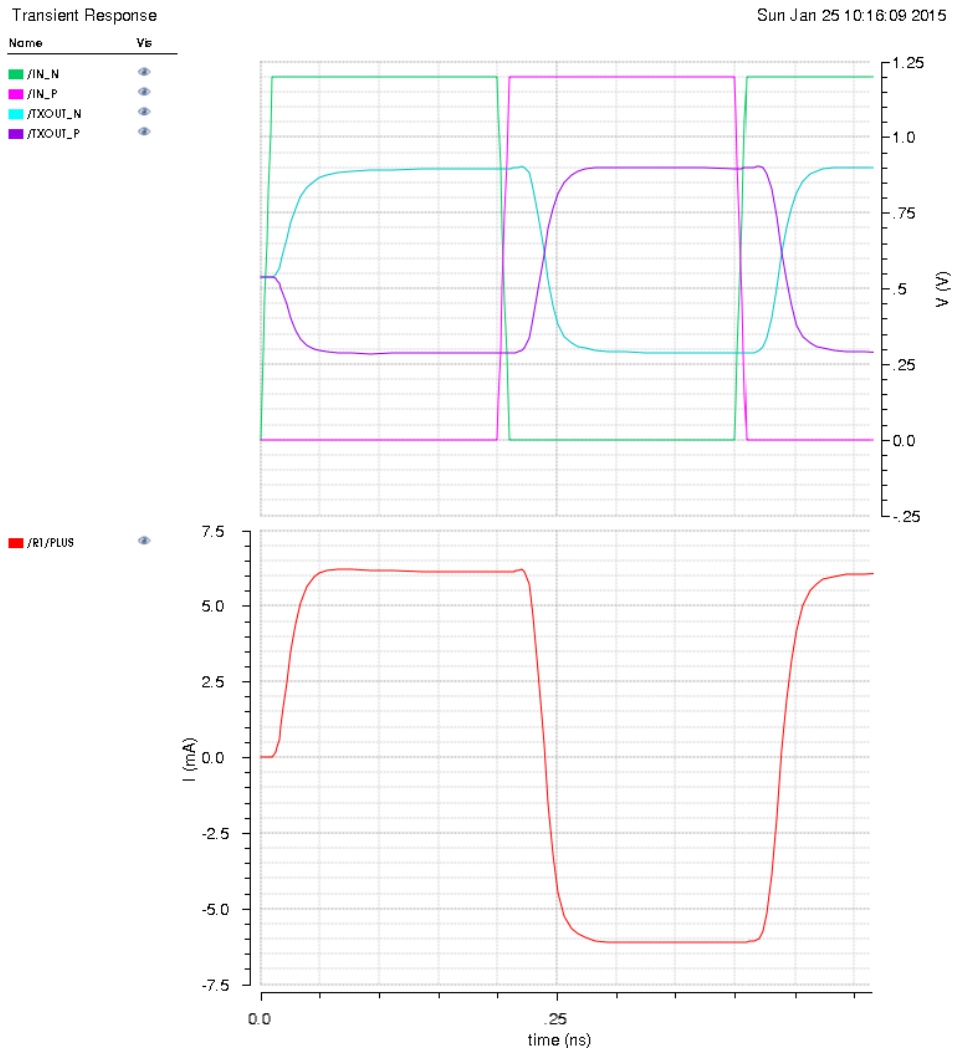


Figure 15 : output real output-stage

Modeling

- Simulation time on transistor level with SPICE need to much time
- Perfect for top-down approach - behavior model will be specified and integrated in test benches
- Information about the model detail required
- Model types
  - device based design (Spectre, SPICE)
  - analog modeling (Verilog-A)
  - mixed-signal modeling (Verilog-AMS)
  - discrete real number modeling(Verilog-AMS)
  - logic modeling(Verilog)

My Task - AMS Behavior Model

- Measure the key parameters of the real output-stage
- Take the measured values and parameterize a AMS-model
- If necessary expand the AMS-model to get an almost identical behavior
- Compare the simulation behavior, accuracy and time consumption

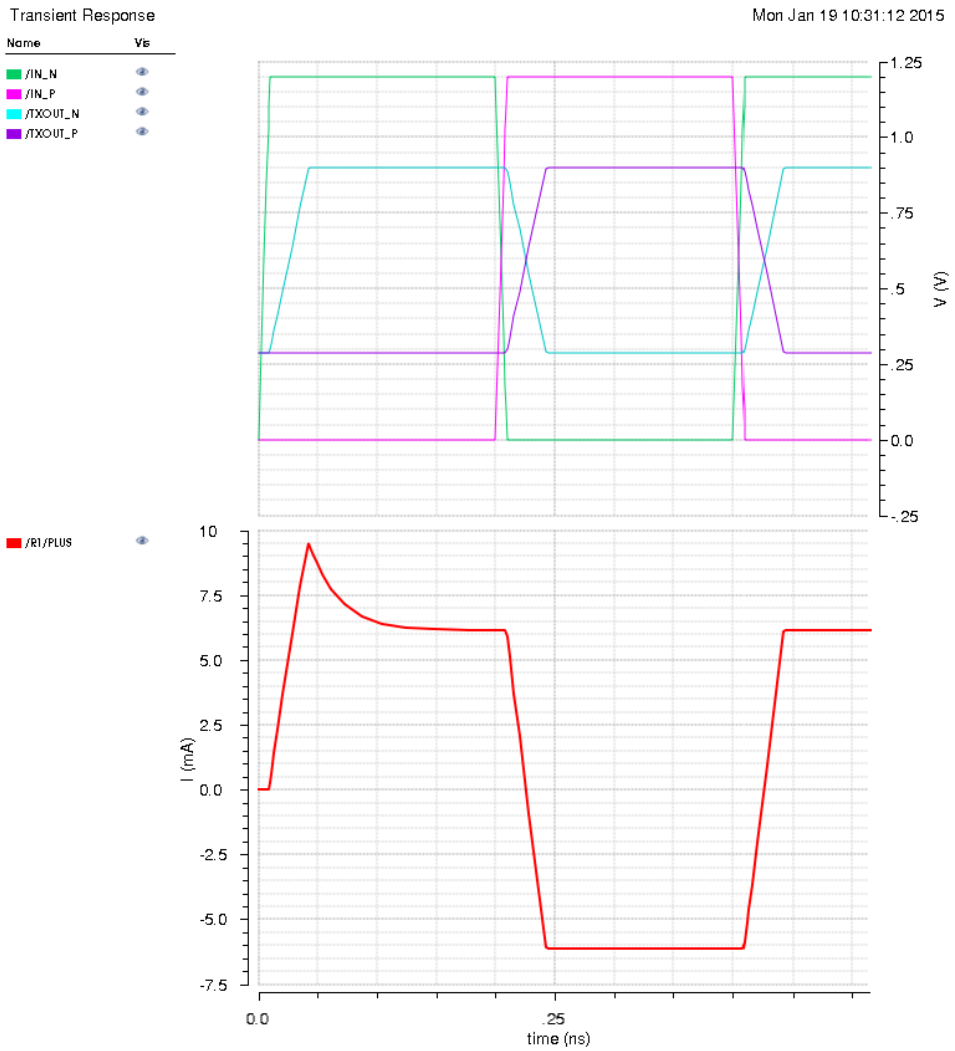


Figure 16 : output model output-stage

Output Stage AMS Model

- Expand with analog sampling of inputs
- Remove the digital filter
- Expand with parametrized high and low output values

```
always  @(above(V(IN_P)-V_HI+0.1))
        begin
                InP_logic <= 1'b1;
        end
```

```
case (InP_logic)
        1'b1:  begin
         VoutP=SW_HI; [...]
        end
        1'b0: begin
         VoutP=SW_LO;[...]
    endcase
```

```
analog begin
  // Rout shifts on log scale
  RoutP = exp(transition(RlogP,
                         0,
                         TrRP,
                         TrRP));
  I(OUT_P) <+
        (V(OUT_P) - transition(VoutP,
                               TdVP,
                               TrVP,
                               TrVP)
        )/RoutP; // linear Vout chg

end
```

Measurements 1/2

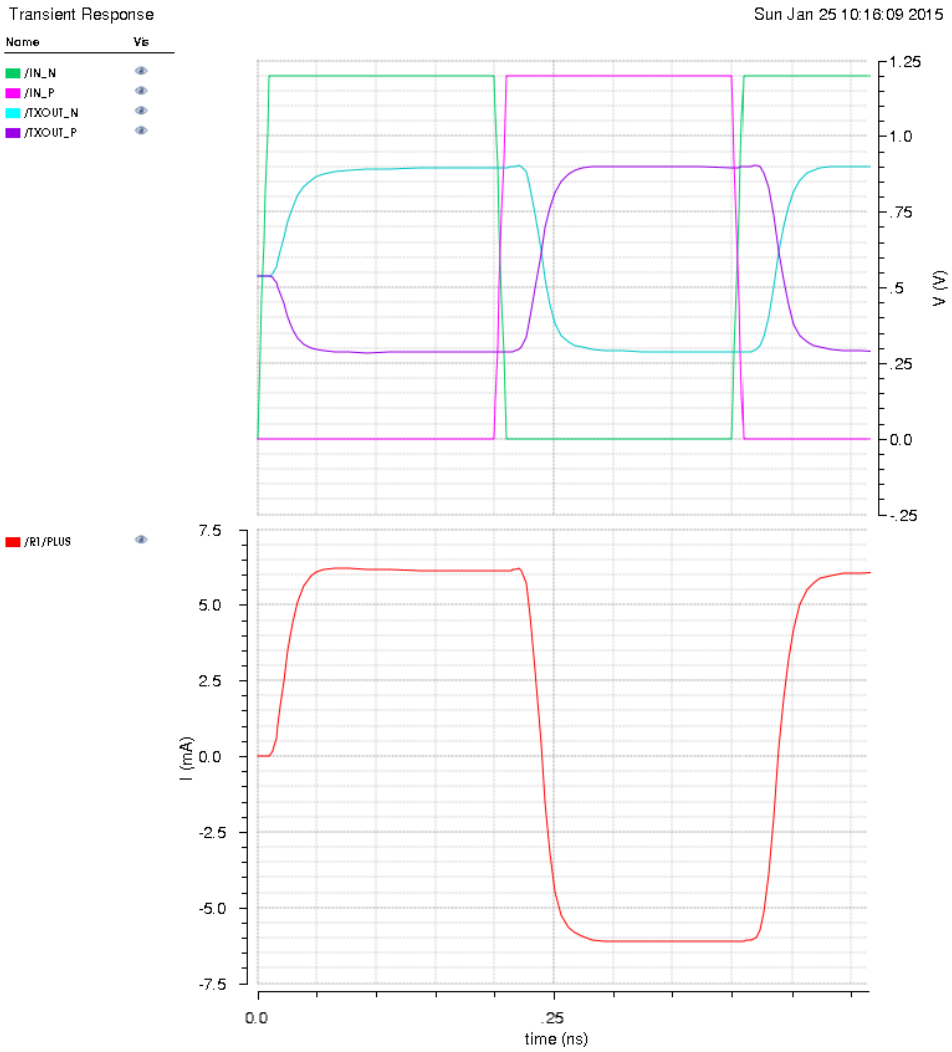


Figure 17 : output real output-stage

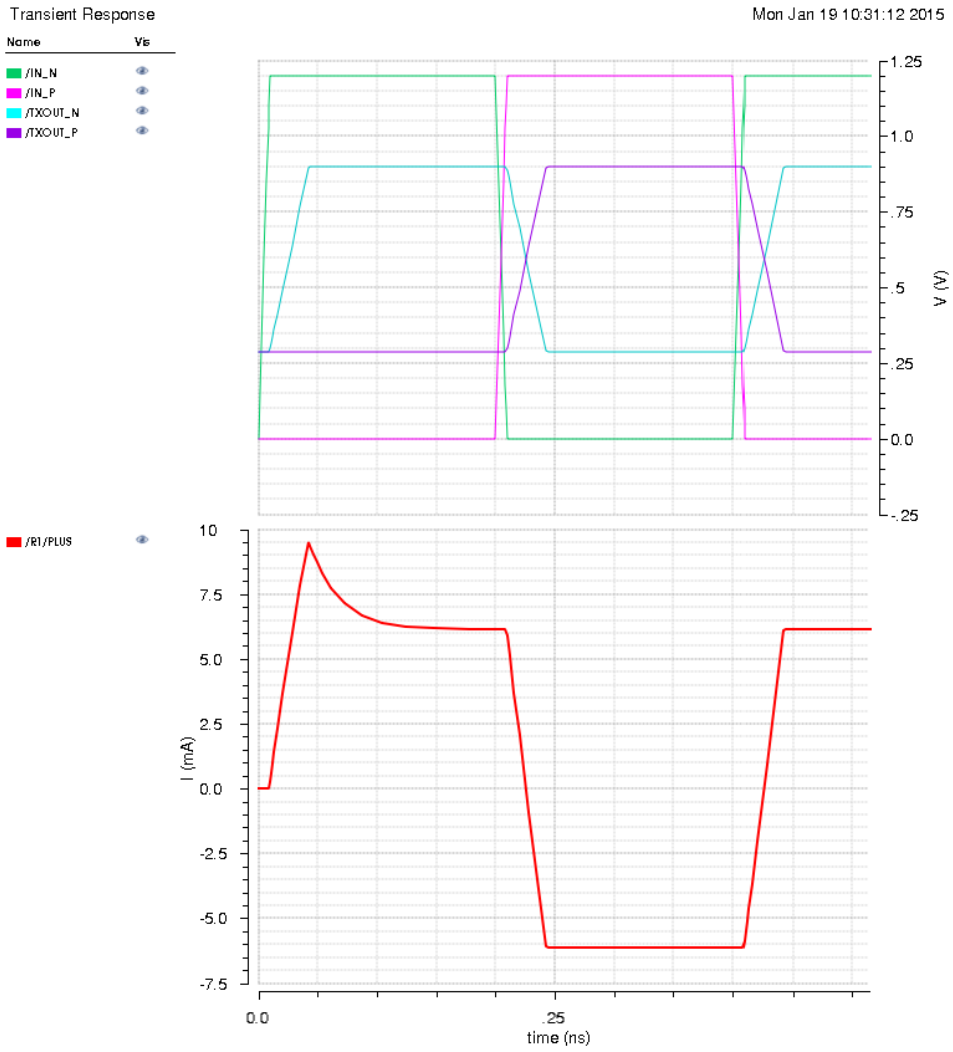
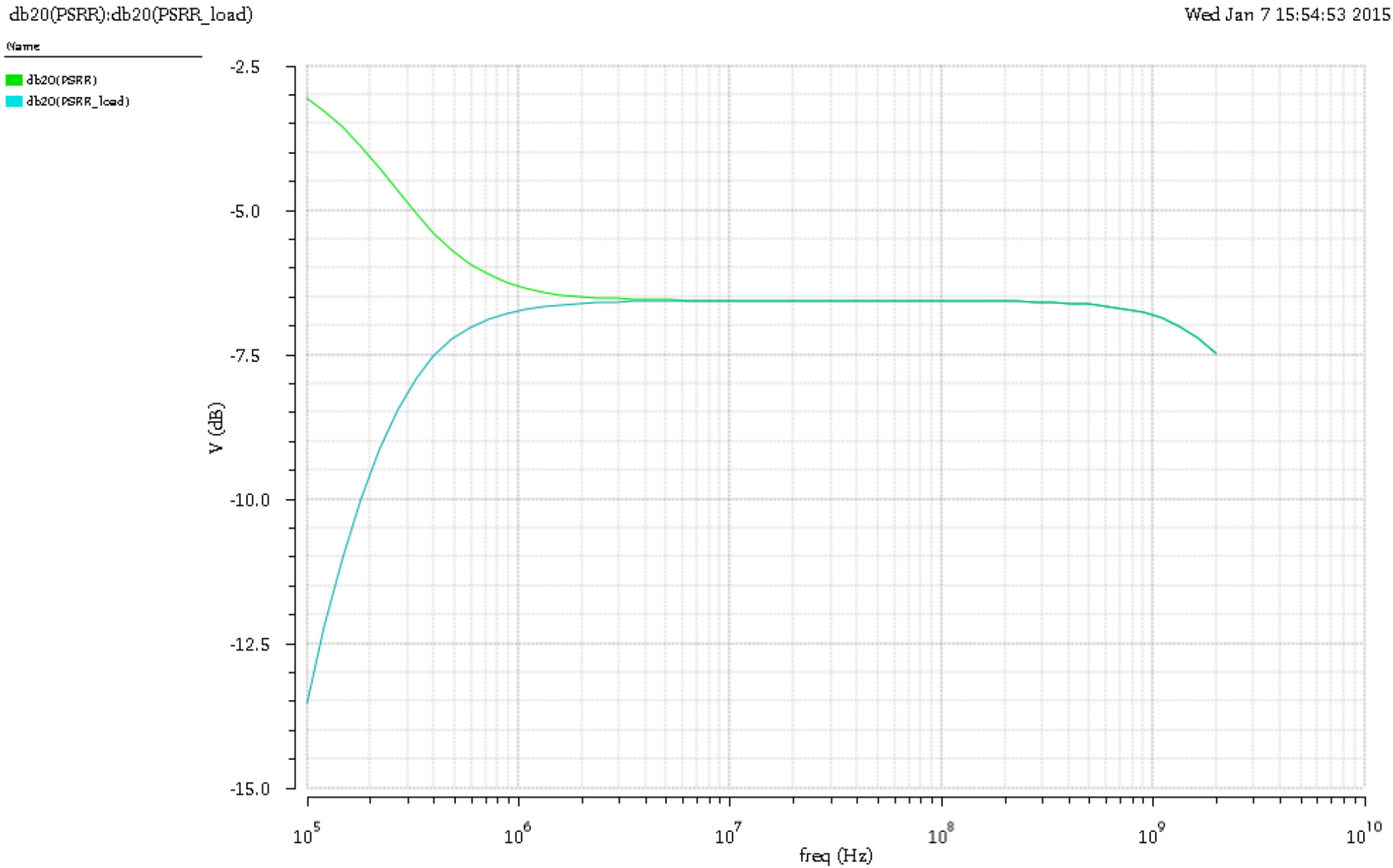


Figure 18 : output model output-stage

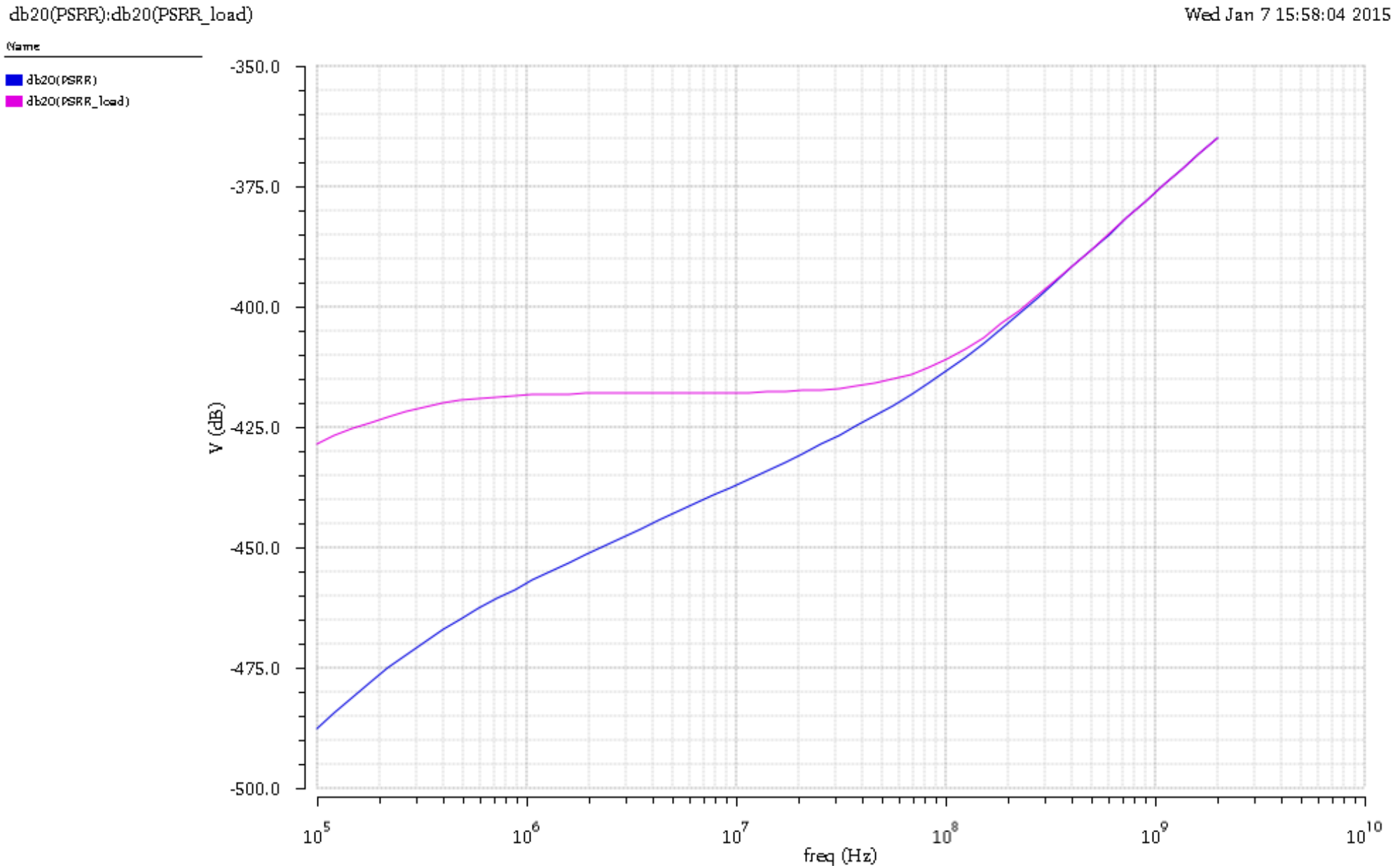
Measurements 2/2

	real output stage		model output stage	
	load 300fF	**load 600 fF**	**load 300fF**	**load 600 fF**
$Voutdiff_{min}[mV]$	-611.9	-610.7	-612.6	-612.8
$Voutdiff_{max}[mV]$	612	610.8	612.8	613
$Tr[ps]$	26.67	36.7	26.57	26.58
$I_{max}[mA]$	37.99	38.45	12.52	17.66
$Pl_{max}[mW]$	3.8	3.76	5.84	5.83
$Pl_{average}[mW]$	3.28	3.09	3.37	3.38
$t_{sim}(4\mu s)[s]$	909.5		19.7	

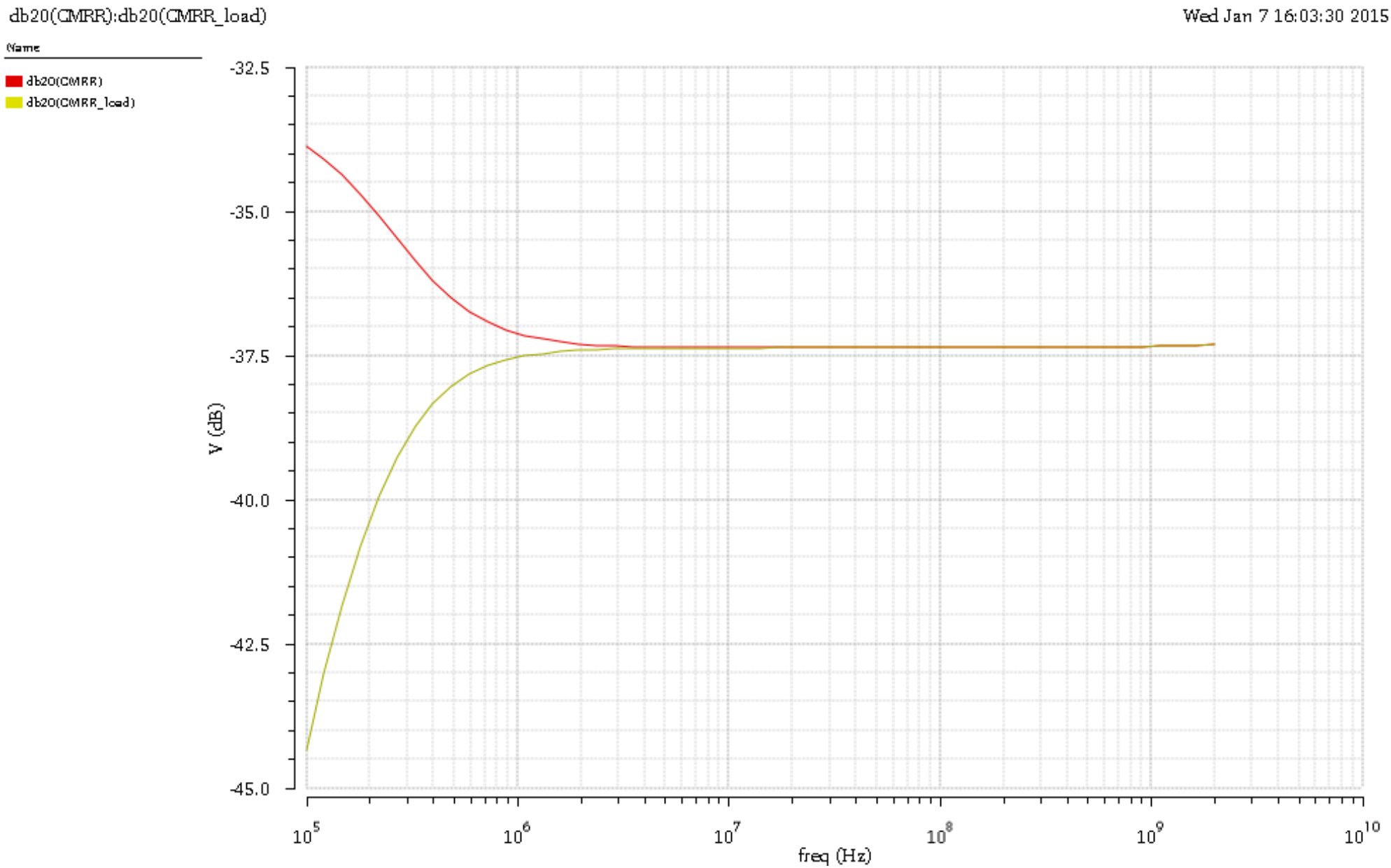
PSRR real output-stage



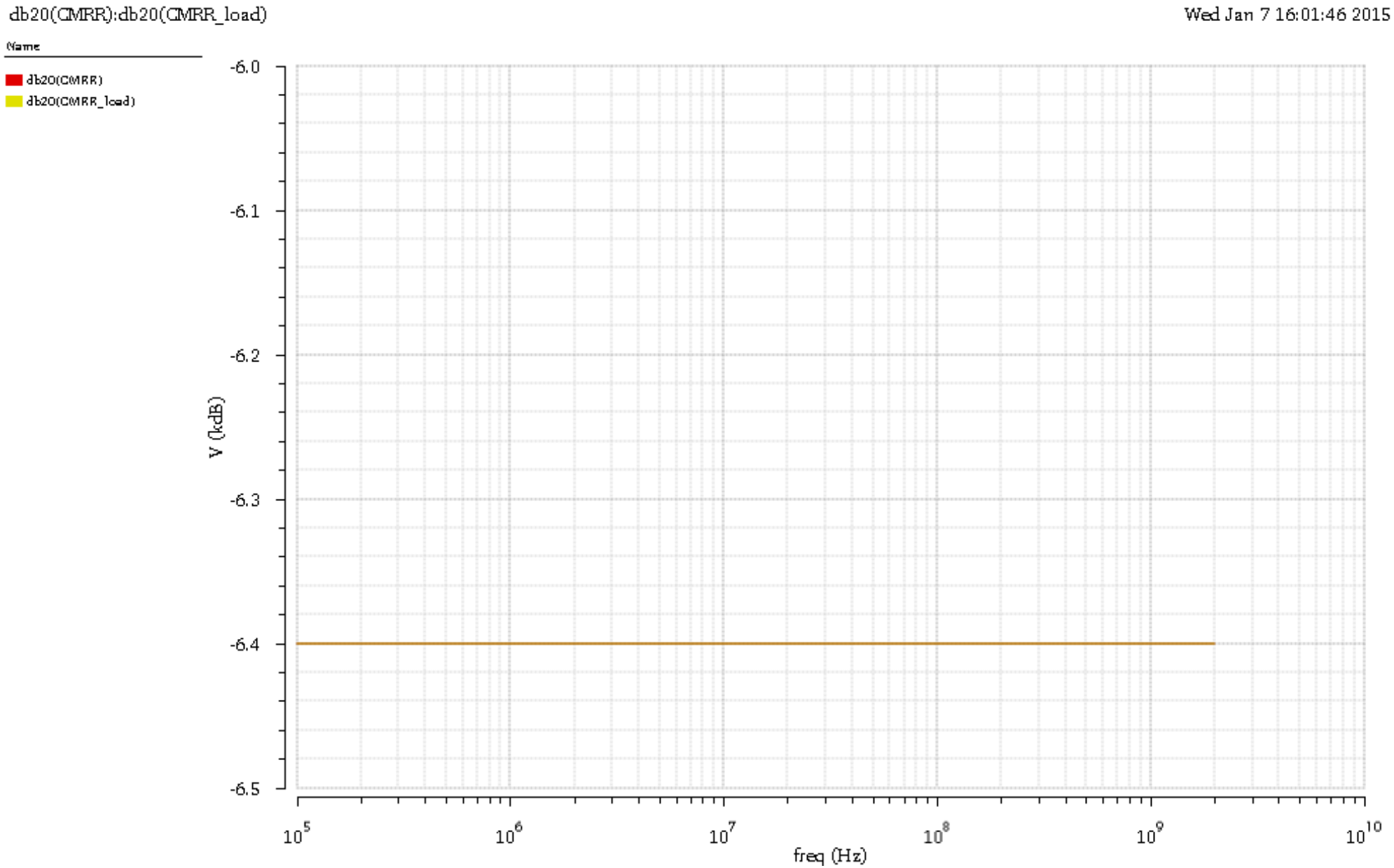
PSRR model output-stage



CMRR real output-stage



CMRR model output-stage



Conclusions of the Measurements

- Model is a strong simplification of the real output stage
  - model has no saturation effect
  - model has no power consumption
  - model has no current limitation
  - model is load and common mode independent
- Faster simulation (speed up ≈ 46.2)
- For real use model should be extended for more accuracy
  $\Rightarrow$less speed-up

Summary and Future Trends

- Trend is towards SoCs
- Mixed-signal design becomes more and more important
- Different methodologies depend on project focus
- Many vendors for commercial EDA and open source solutions
- Use of analog IP could lead to problems in verification
- Modeling of analog functions to reduce verification time
  $\Rightarrow$ tightrope walk between speed and accuracy

References I

[1] [Online]. Available: http://www.customsiliconsolutions.com/products-for-ASIC-solutions/basics-products.aspx

[2] [Online]. Available: http://www.righto.com/2014/10/how-z80s-registers-are-implemented-down.html

[3] [Online]. Available: http://www.semiconductor-today.com/news_items/2014/AUG/KTH_010814.shtml

[4] [Online]. Available: http://en.wikipedia.org/wiki/Analog_signal

[5] [Online]. Available: https://www.ifixit.com/Teardown/Apple+A6+Teardown/10528

[6] V. Grimblatt, "Synthesis - state of art," in *Devices, Circuits and Systems, Proceedings of the 6th International Caribbean Conference on*, April 2006, pp. 327–332.

[7] O. O'Riordan. (2013, December) Mixed signal design & verification methodology for complex socs. S3 Group, Silicon Business. [Online]. Available: http://www.s3group.com/silicon/resource-center/download/dlitem/129/

[8] J. Chen, M. Henrie, M. Mar, and M. Nizic, *Mixed-Signal Methodology Guide*. Cadence Design Systems, Incorporated, 2012. [Online]. Available: https://books.google.de/books?id=RKrfAwAAQBAJ

[9] [Online]. Available: http://en.wikipedia.org/wiki/Verilog

[10] [Online]. Available: http://en.wikipedia.org/wiki/SystemVerilog

[11] [Online]. Available: http://www.williamson-labs.com/480_opam.htm

[12] (2012, Janurary) Custom and mixed-signal design solution unified solution for custom and cell-based design and verification. Synopsys. [Online]. Available: http://www.synopsys.com/Tools/Implementation/Documents/custom-design-solution-overview.pdf

[13] [Online]. Available: http://www.cadence.com/solutions/ms/Pages/ms_implementation.aspx

[14] [Online]. Available: http://www-soc.lip6.fr/en/

[15] [Online]. Available: http://wiki.geda-project.org/geda:faq

[16] [Online]. Available: http://opencircuitdesign.com/

I look forward to the discussion round